ITRS-2001 Overview

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What is the ITRS? (public.itrs.net)

- Sets requirements for semiconductor industry supplier chain
  - Lithography, Process Integration, Test, Assembly & Packaging, Design, Interconnect, Front-End Processing, Environmental Safety & Health, Factory Integration, …
  - Without such coordination, semiconductor industry cannot progress
- Collaborative effort
  - 5+ regional industry regional roadmapping associations (Japan, Taiwan, Europe, U.S., Korea) and multiple sub-associations
  - 800+ individual contributors to 2001 ITRS
- Schedule
  - Odd years: "Renewal" (new edition)
  - Even years: "Update" (smaller changes)
  - Three conferences each year: March-April (Europe), July (USA), December (Asia)
- Tensions
  - Competition
  - "Requirement" vs. "Prediction"
  - Constraints (pure technology, vs. cost feasibility)

Outline

- Overall Roadmap Technology Characteristics
- System Drivers
- Process Integration, Devices and Structures
- Lithography
- Interconnect
- Assembly and Packaging
- Design

ITRS-2001 Overall Roadmap Technology Characteristics

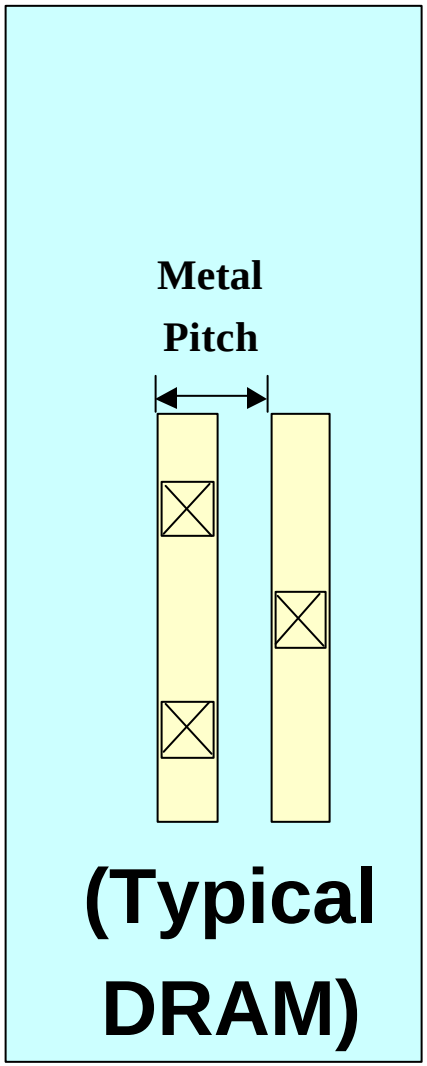
MOS Transistor Scaling (1974 to present)

S=0.7

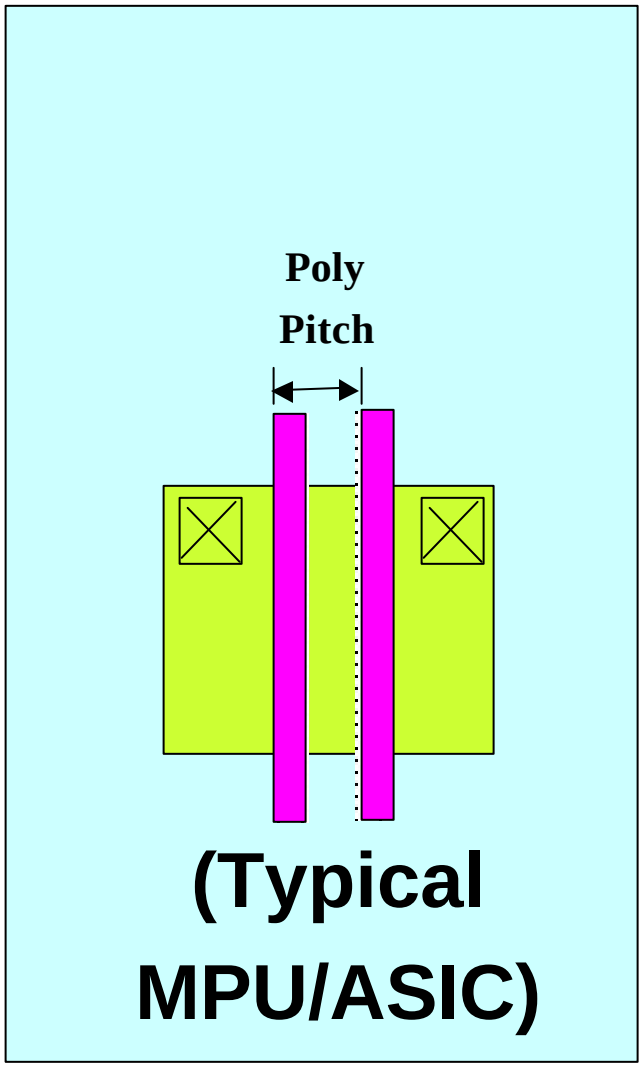
[0.5x per 2 nodes]

Source: 2001 ITRS - Exec. Summary, ORTC Figure

Half Pitch (= Pitch/2) Definition



(Typical DRAM)



(Typical MPU/ASIC)

Source: 2001 ITRS - Exec. Summary, ORTC Figure

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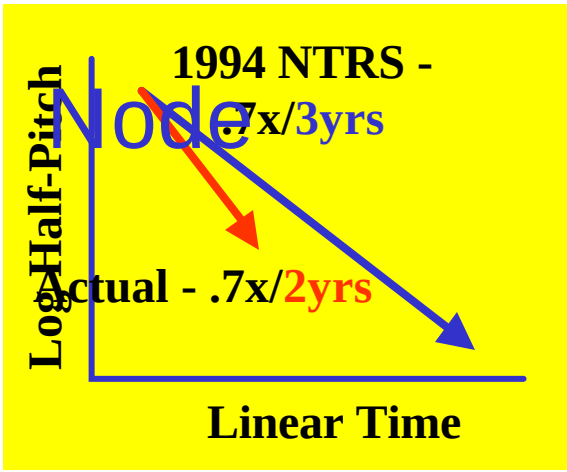
Back to Basics

Technology Nodes (nm)

WAS		X		IS	Actual	%
100	130	X	0.7	91	90	-10.00
70	90	X	0.7	64	65	-7.14
50	65	X	0.7	45	45	-10.00
35	45	X	0.7	31	32	-8.57
25	32	X	0.7	22	22	-12.00

Scaling Calculator + Node Cycle Time:



0.7x 0.7x

250 -> 180 -> 130 -> 90 -> 65 -> 45 -> 32 -> 22 -> 16

0.5x

N N+1 N+2

* CARR(T) = Compound Annual Reduction Rate (@ cycle time period, T)

Node Cycle Time (T yrs):

*CARR(T) =

[(0.5)^(1/2T yrs)] - 1

CARR(3 yrs) = -10.9%

CARR(2 yrs) = -15.9%

Source: 2001 ITRS - Exec. Summary, ORTC Figure

2001 ITRS

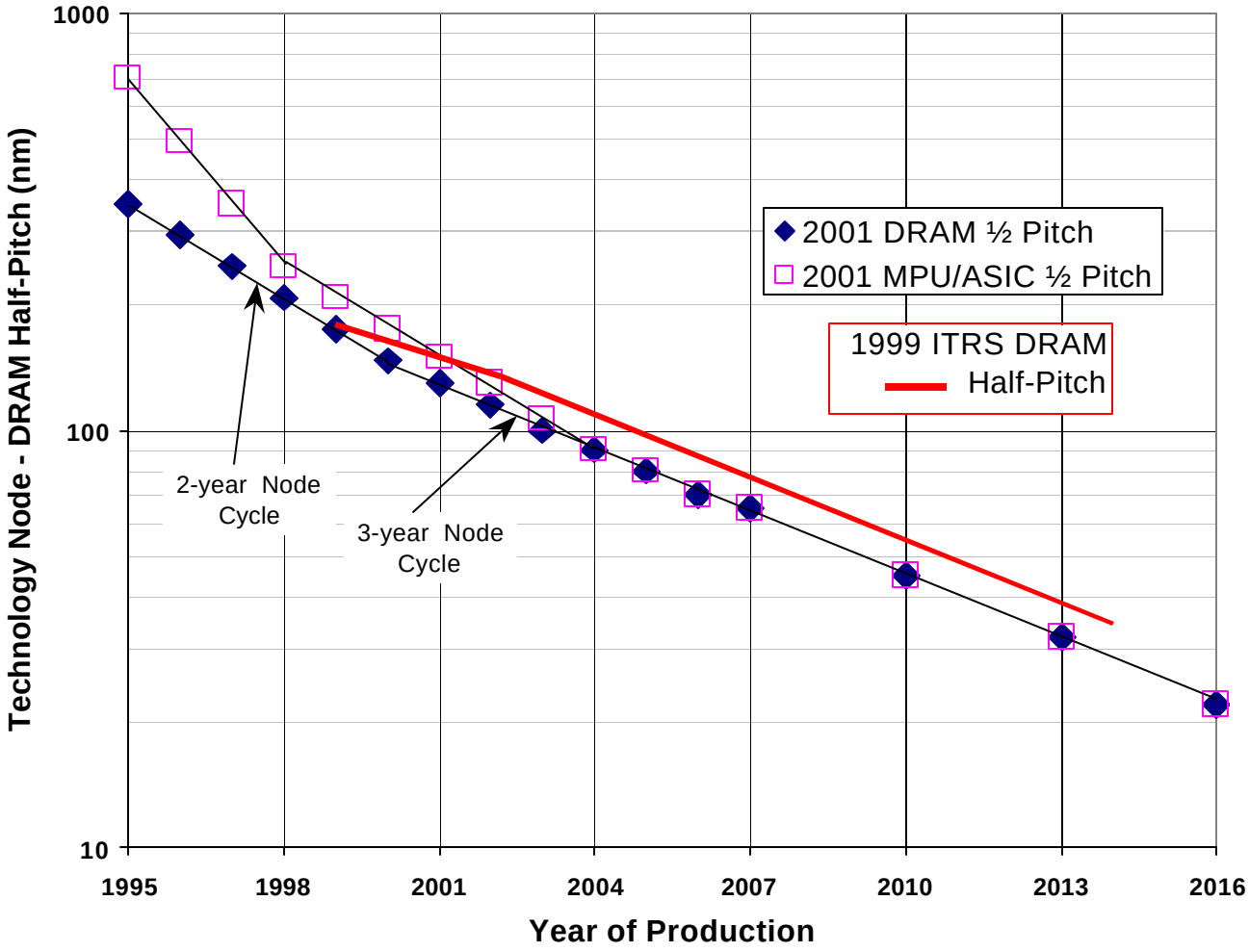
Timing Highlights

- **The DRAM Half-Pitch (HP) remains on a 3-year-cycle trend after 130nm/2001**
- **The MPU/ASIC HP remains on a 2-year-cycle trend until 90nm/2004, and then remains equal to DRAM HP (3-year cycle)**

- **The MPU Printed Gate Length (Pr GL) and Physical Gate Length (Ph GL) will be on a 2-year-cycle until 45nm and 32nm, respectively, until the year 2005**
- **The MPU Pr GL and Ph GL will proceed parallel to the DRAM/MPU HP trends on a 3-year cycle beyond the year 2005**

- **The ASIC/Low Power Pr/Ph GL is delayed 2 years behind MPU Pr/Ph GL**
- **ASIC HP equal to MPU HP**

ITRS Roadmap Acceleration Continues...Half Pitch



Source: 2001 ITRS - Exec. Summary, ORTC Figure

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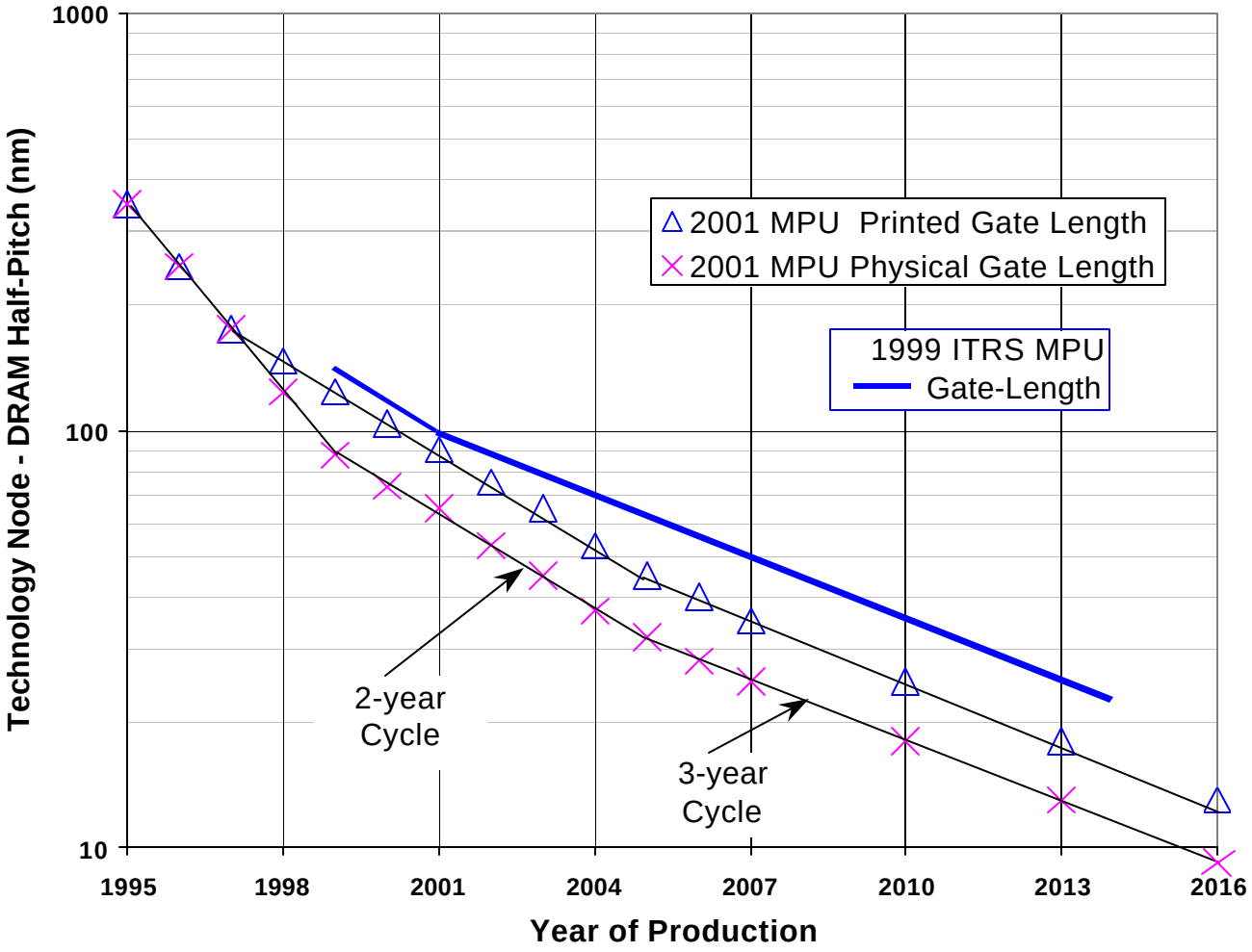
ITRS Roadmap Acceleration Continues…Gate Length



Source: 2001 ITRS - Exec. Summary, ORTC Figure

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2001 ITRS ORTC Node Tables

Table 1a Product Generations and Chip Size Model Technology Nodes—Near-term Years

YEAR OF PRODUCTION	2001	2002	2003	2004	2005	2006	2007
DRAM ½ Pitch (nm)	130	115	100	90	80	70	65
MPU/ASIC ½ Pitch (nm)	150	130	107	90	80	70	65
MPU Printed Gate Length (nm) ††	90	75	65	53	45	40	35
MPU Physical Gate Length) (nm)	65	53	45	37	32	28	25
ASIC/Low Power Printed Gate Length (nm) ††	130	107	90	75	65	53	45
ASIC/Low Power Physical Gate Length) (nm)	90	75	65	53	45	37	32

Table 1b Product Generations and Chip Size Model Technology Nodes—Long-term years

YEAR OF PRODUCTION	2010	2013	2016
DRAM ½ Pitch (nm)	45	32	22
MPU/ASIC ½ Pitch (nm)	45	32	22
MPU Printed Gate Length (nm) ††	25	18	13
MPU Physical Gate Length) (nm)	18	13	9
ASIC/Low Power Printed Gate Length (nm) ††	32	22	16
ASIC/Low Power Physical Gate Length) (nm)	22	16	11

Source: 2001 ITRS - Exec. Summary, ORTC Table

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2001 ITRS ORTC MPU Frequency Tables

Table 4c Performance and Package Ch ips: Frequency On -Chip Wiring Levels — Near -Term Years

EAR OF PRODUCTION	2001	2002	2003	2004	2005	2006	2007
DRAM ½ Pitch (nm)	130	115	100	90	80	70	65
MPU/ASIC ½ Pitch (nm)	150	130	107	90	80	70	65
MPU Printed Gate Length (nm)	90	75	65	53	45	40	35
MPU Physical Gate Length (nm)	65	53	45	37	32	28	25
hip Frequency (MHz)							
n-chip local clock	1,684	2,317	3,088	3,990	5,173	5,631	6,739
hip-to-board (off-chip) speed igh-performance, for peripheral buses)[1]	1,684	2,317	3,088	3,990	5,173	5,631	6,739
laximum number wiring levels—maximum	7	8	8	8	9	9	9
laximum number wiring levels—minimum	7	7	8	8	8	9	9

Table 4d Performance and Package Chips: Frequency, On -Chip Wiring Levels—Long-term Years

YEAR OF PRODUCTION	2010	2013	2016
DRAM ½ Pitch (nm)	45	32	22
MPU/ASIC ½ Pitch (nm)	45	32	22
MPU Printed Gate Length (nm)	25	18	13
MPU Physical Gate Length (nm)	18	13	9
Chip Frequency (MHz)			
On-chip local clock	11,511	19,348	28,751
Chip-to-board (off-chip) speed (high-performance, for peripheral buses)[1]	11,511	19,348	28,751
Maximum number wiring levels—maximum	10	10	10
Maximum number wiring levels—minimum	9	9	10

Source: 2001 ITRS - Exec. Summary, ORTC Table

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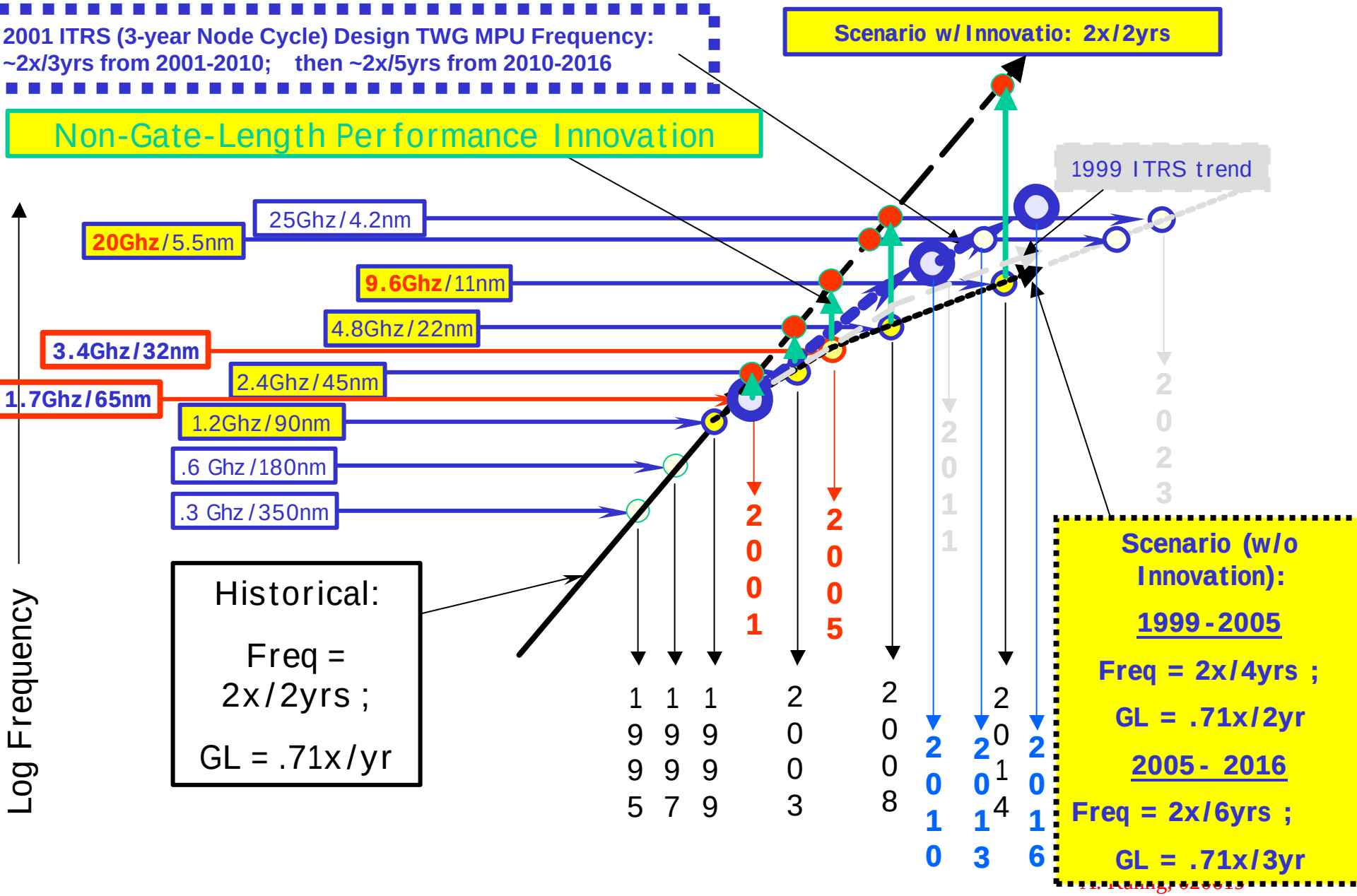
MPU Max Chip Frequency – 2001 ITRS Design TWG Model vs 1999 ITRS, and 2000 Update Scenario "w/o Innovation"



What Is A “Red Brick” ?

- Red Brick = ITRS Technology Requirement with no known solution

- Alternate definition: Red Brick = something that REQUIRES billions of dollars in R&D investment

The "Red Brick Wall" - 2001 ITRS vs 1999

Table 1. 2001 Status of Red Brick Wall

Year of production	2001	2003	2005		2007	2010	2016
DRAM half-pitch (nm)	130	100	80		65	45	22
Overlay accuracy (nm)	46	35	28		23	18	9
MPU gate length (nm)	90	65	45		35	25	13
CD control (nm)	8	5.5	3.9		3.1	2.2	1.1
T_{ox} (equivalent) (nm)	1.3-1.6	1.1-1.6	0.8-1.3		0.6-1.1	0.5-0.8	0.4-0.5
Junction depth (nm)	48-95	33-66	24-47		18-37	13-26	7-13
Metal cladding thickness (nm)	16	12	9		7	5	2.5
Intermetal dielectric constant, k	3.0-3.6	3.0-3.6	2.6-3.1		2.3-2.7	2.1	1.8

Table 2. 1999 Status of Red Brick Wall

Year of production	1999	2002	2005		2008	2011	2014
DRAM half-pitch (nm)	180	130	100		70	50	35
Overlay accuracy (nm)	65	45	35		25	20	15
MPU gate length (nm)	140	85-90	65		45	30-32	20-22
CD control (nm)	14	9	6		4	3	2
T_{ox} (equivalent) (nm)	1.9-2.5	1.5-1.9	1.0-1.5		0.8-1.2	0.6-0.8	0.5-0.6
Junction depth (nm)	42-70	25-43	20-33		16-26	11-19	8-13
Metal cladding thickness (nm)	17	13	10		0	0	0
Intermetal dielectric constant, k	3.5-4.0	2.7-3.56	1.6-2.2		1.5	<1.5	<1.5

Source: Semiconductor International - http://www.e-insite.net/semiconductor/index.asp?layout=article&articleId=CA187876

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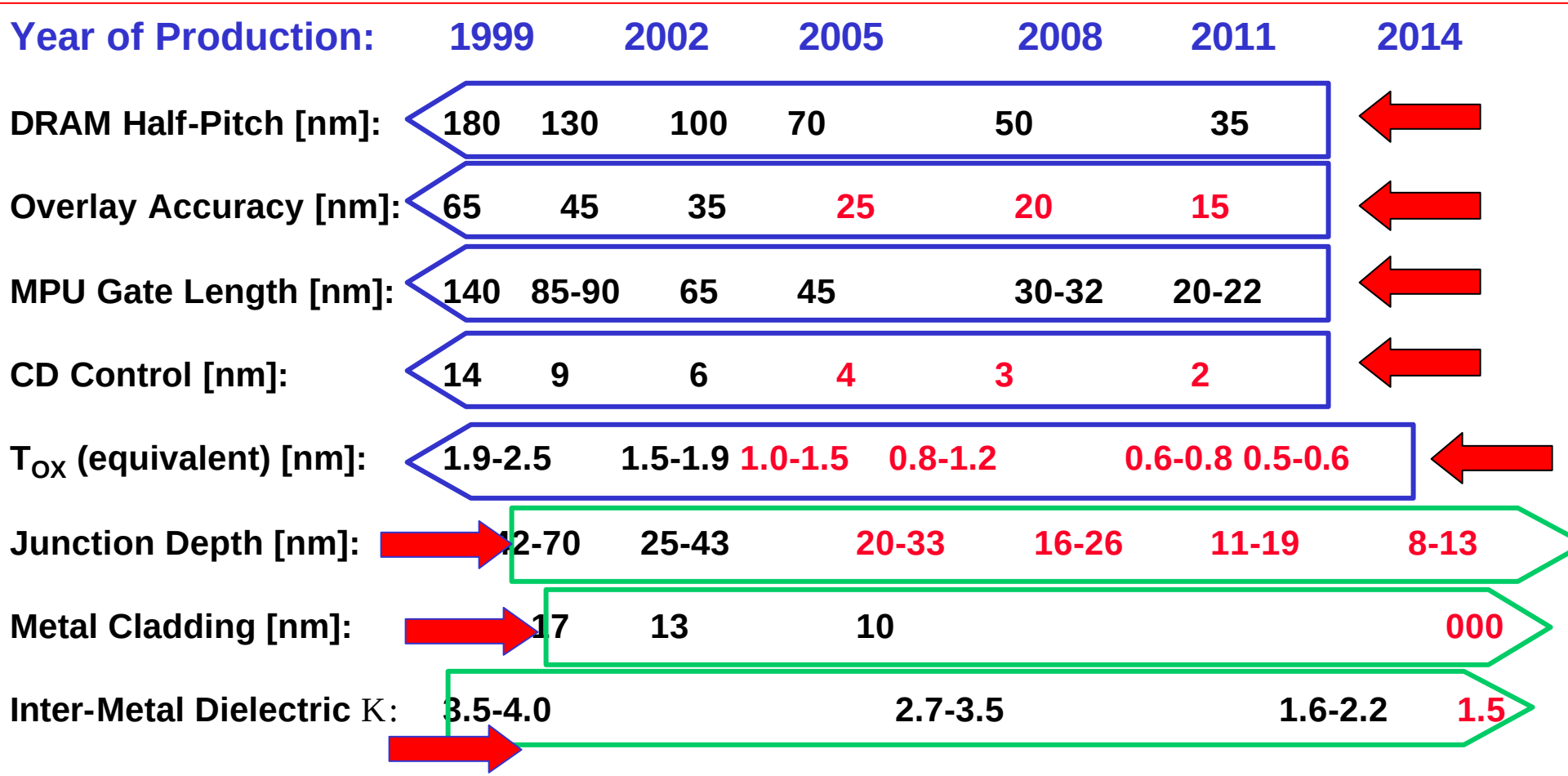
Roadmap Acceleration and Deceleration

2001 versus 1999 Results



Source: A. Allan, Intel

Summary

- New Technology Nodes defined
- Technology acceleration (2-year cycle) continues in 2001 ITRS
- Gate length reduction proceeding faster than pitch reduction (until 2005)
- DRAM half-pitch is expected to return to a 3-year cycle after 2001 but….*so we have said before*
- DRAM and MPU half-pitch dimensions will merge in 2004
- Innovation will be necessary, in addition to technology acceleration, to maintain historical performance trends

ITRS-2001 System Drivers Chapter

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System Drivers Chapter

- Defines the IC products that drive manufacturing and design technologies
- Replaces the 1999 SOC Chapter

- Goal: ORTCs + System Drivers = “consistent framework for technology requirements”

- Starts with macro picture
  - Market drivers
  - Convergence to SOC
- Main content: System Drivers
  - MPU – traditional processor core
  - SOC – focus on low-power “PDA” (and, high-speed I/O)
  - AM/S – four basic circuits and Figures of Merit
  - DRAM – not developed in detail

MPU Driver

- Two MPU flavors
  - Cost-performance: constant 140 mm^2 die, "desktop"
  - High-performance: constant 310 mm^2 die, "server"
  - (Next ITRS: merged desktop-server, mobile flavors ?)
  - MPU organization: multiple cores, on-board L3 cache
    - More dedicated, less general-purpose logic
    - More cores help power management (lower frequency, lower Vdd, more parallelism → overall power savings)
    - Reuse of cores helps design productivity
    - Redundancy helps yield and fault-tolerance
    - MPU and SOC converge (organization and design methodology)
- No more doubling of clock frequency at each node

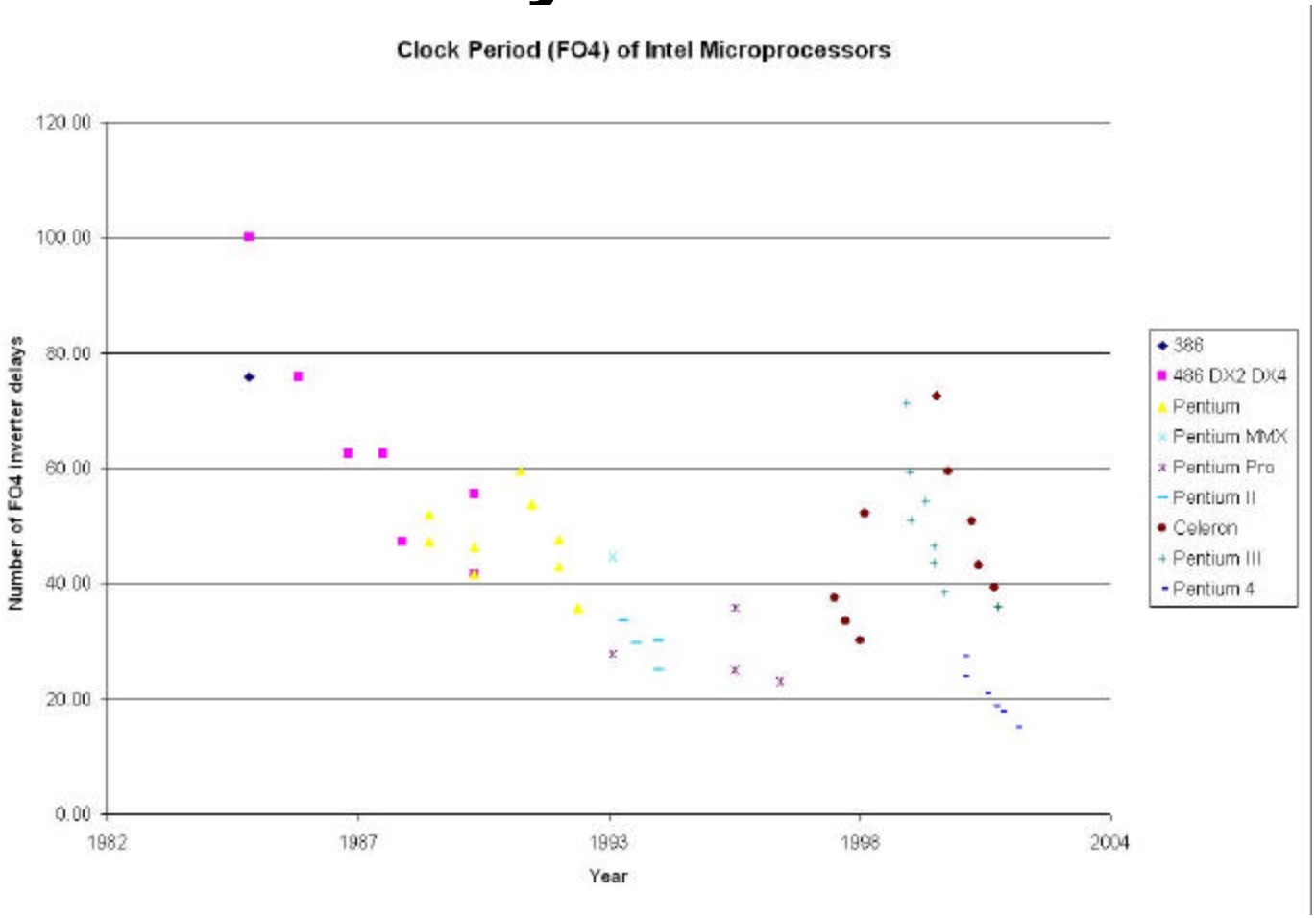
Example Supporting Analyses (MPU)

- Logic Density: Average size of 4t gate = $32MP^2 = 320F^2$
  - MP = *lower-level contacted metal pitch*
  - F = half-pitch (technology node)
  - 32 = 8 tracks standard-cell height times 4 tracks width (average NAND2)
  - Additional whitespace factor = 2x (i.e., 100% overhead)
  - Custom layout density = 1.25x semi-custom layout density
- SRAM (used in MPU) Density:
  - **bitcell area (units of F^2) near flat: 223.19*F (um) + 97.748**
  - peripheral overhead = 60%
  - memory content is increasing (driver: power) and increasingly fragmented
  - **Caveat:** shifts in architecture/stacking; eDRAM, 1T SRAM, 3D integ
- Density changes affect power densities, logic-memory balance
  - **130nm : 1999 ASIC logic density = 13M tx/cm^2, 2001 = 11.6M tx/cm^2**
  - **130nm : 1999 SRAM density = 70M tx/cm2, 2001 = 140M tx/cm^2**

Example Supporting Analyses (MPU)

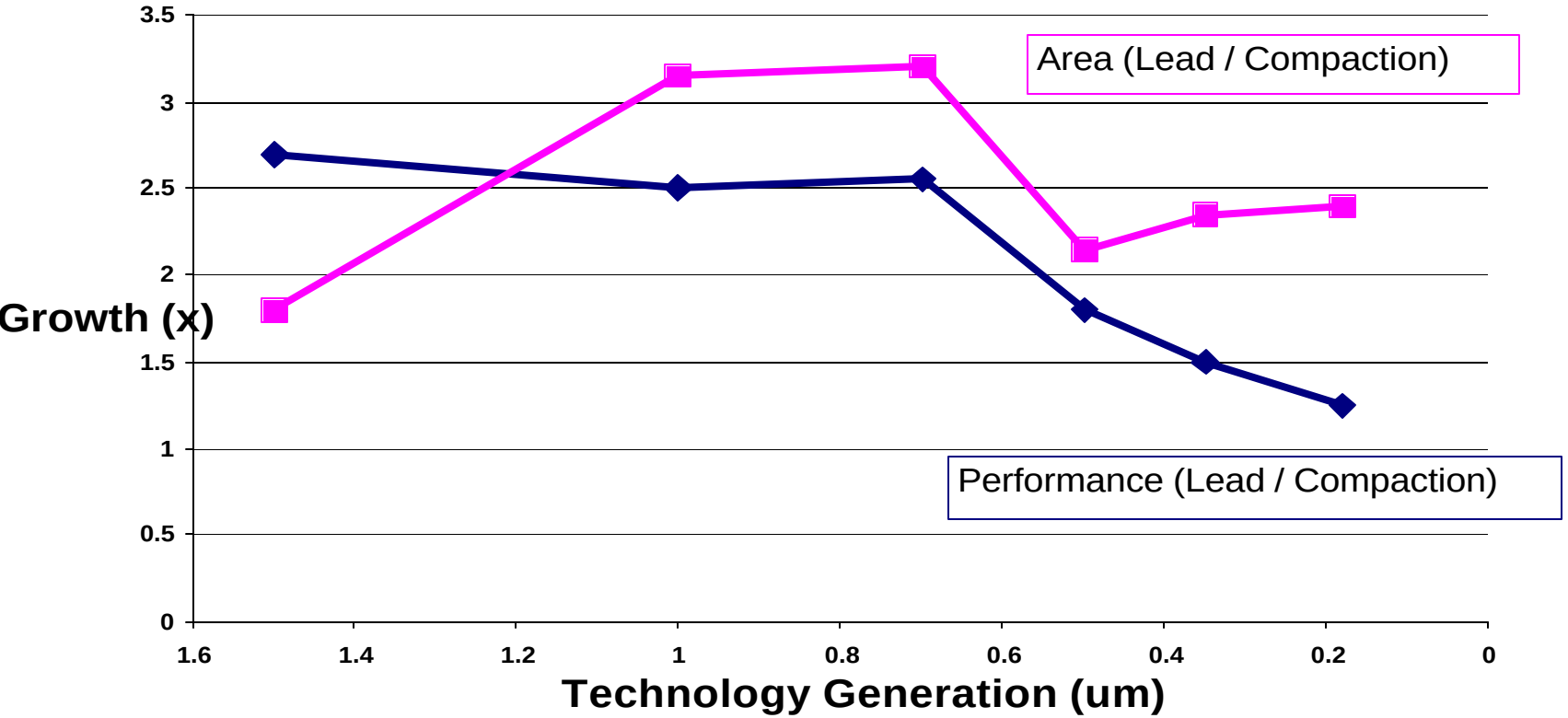
- Diminishing returns
  - "Pollack's Rule": In a given node, new microarchitecture takes 2-3x area of previous generation one, but provides only 50% more performance
  - "Law of Observed Functionality": transistors grow exponentially, while utility grows linearly
- Power knob running out
  - Speed from Power: scale voltage by 0.85x instead of 0.7x per node
  - Large switching currents, large power surges on wakeup, IR drop issues
  - Limited by Assembly and Packaging roadmap (bump pitch, package cost)
  - Power management: 25x improvement needed by 2016
- Speed knob running out
  - Where did 2x freq/node come from? 1.4x scaling, 1.4x fewer logic stages
  - But clocks cannot be generated with period < 6-8 FO4 INV delays
  - Pipelining overhead (1-1.5 FO4 delay for pulse-mode latch, 2-3 for FF)
  - ~14-16 FO4 delays = practical limit for clock period in core (L1$, 64b add)
  - **Cannot continue 2x frequency per node trend**

FO4 INV Delays Per Clock Period



- FO4 INV = inverter driving 4 identical inverters (no interconnect)
- Half of freq improvement has been from reduced logic stages

Diminishing Returns: Pollack's Rule



- Area of "lead" processor is 2-3X area of "shrink" of previous generation processor
- Performance is only 1.5X better

SOC Low-Power Driver Model (STRJ)

ear of Products	2001	2004	2007	2010	2013	2016
rocess Technology (nm)	130	90	65	45	32	22
peration Voltage (V)	1.2	1	0.8	0.6	0.5	0.4
lock Frequency (MHz)	150	300	450	600	900	1200
pplication	Still Image Processing	Real Time Video Code		Real Time Interpretation		
MAX performance required)		(MPEG4/CIF)				
pplication	Web Browser	TV Telephone (1:1)		TV Telephone (>3:1)		
Others)	Electric Mailer	Voice Recognition (Input)		Voice Recognition (Operation)		
	Scheduler	Authentication (Crypto Engine)				
rocessing Performance (GOPS)	0.3	2	15	103	720	5042
ommunication Speed (Kbps)	64	384	2304	13824	82944	497664
ower Consumption (mW/MOPS)	0.3	0.2	0.1	0.03	0.01	0.006
eak Power Consumption (W)	0.1	0.3	1.1	2.9	10.0	31.4
Requirement)		0.1	0.1	0.1	0.1	0.1
tandby power consumption (mW)	2.1	2.1	2.1	2.1	2.1	2.1
ddressable System Memory (Gb)	0.1	1	10	100	1000	10000

- SOC-LP “PDA” **system**
  - Composition: CPU cores, embedded cores, SRAM/eDRAM
  - Requirements: IO bandwidth, computational power, GOPS/mW, die size
- Drives PIDS/FEP LP device roadmap, Design power management challenges, Design productivity challenges

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Key SOC-LP Challenges

- Power management challenge
  - Above and beyond low-power process innovation
  - Hits SOC before MPU
  - Need slower, less leaky devices: low-power lags high-perf by 2 years
  - Low Operating Power and Low Standby Power flavors → design tools handle multi (Vt,Tox,Vdd)
- Design productivity challenge
  - Logic increases 4x per node; die size increases 20% per node

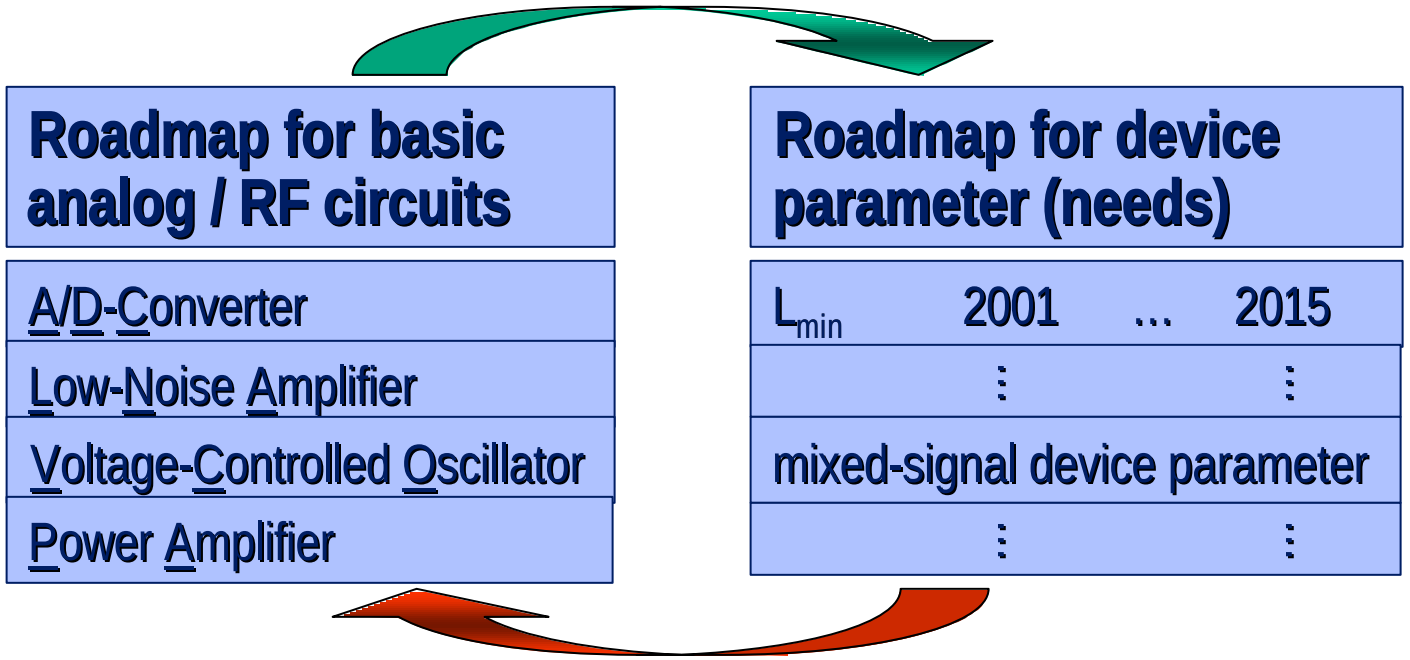
Year	2001	2004	2007	2010	2013	2016
½ Pitch	130	90	65	45	32	22
Logic Mtx per designer-year	1.2	2.6	5.9	13.5	37.4	117.3
Dynamic power reduction (X)	0	1.5	2.5	4	7	20
Standby power reduction (X)	2	6	15	39	150	800

Mixed-Signal Driver (Europe)

- Today, the digital part of circuits is most critical for performance and is dominating chip area
- But in many new IC-products the mixed-signal part becomes important for performance and cost
- This shift requires definition of the “analog boundary conditions” in the design part of the ITRS
- Goal: define criteria and needs for future analog/RF circuit performance, and compare to device parameters:
  - Choose critical, important analog/RF circuits
  - Identify circuit performance needs
  - *and* related device parameter needs

Concept for the Mixed-Signal Roadmap

- Figures of merit for four basic analog building blocks are defined and estimated for future circuit design
- From these figures of merit, related future device parameter needs are estimated (PIDS Chapter table, partially owned by Design)

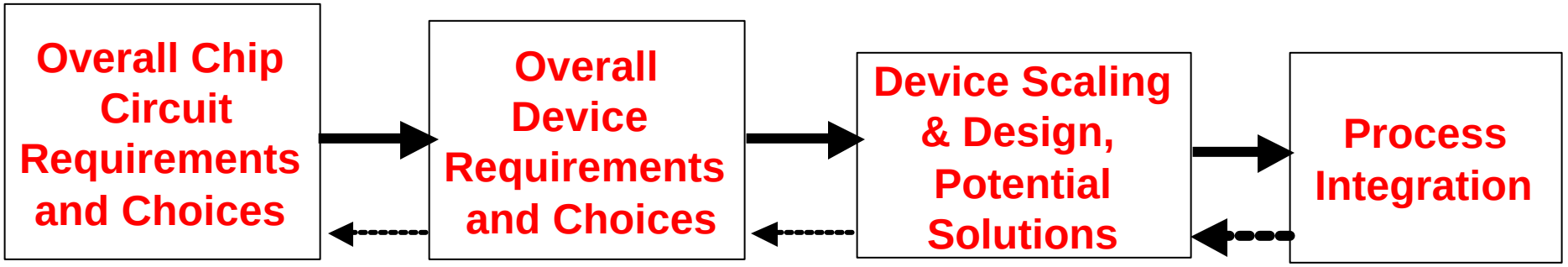


Summary: ANALOGY #1 (?)

- ITRS is like a car
- Before, two drivers (husband = MPU, wife = DRAM)
- The drivers looked mostly in the rear-view mirror (destination = “Moore’s Law”)
- Many passengers in the car (ASIC, SOC, Analog, Mobile, Low-Power, Networking/Wireless, …) wanted to go different places
- This year:
  - Some passengers became drivers
  - All drivers explain more clearly where they are going

ITRS-2001 Process Integration, Devices and Structures (PIDS)

Hierarchy of IC Requirements and Choices



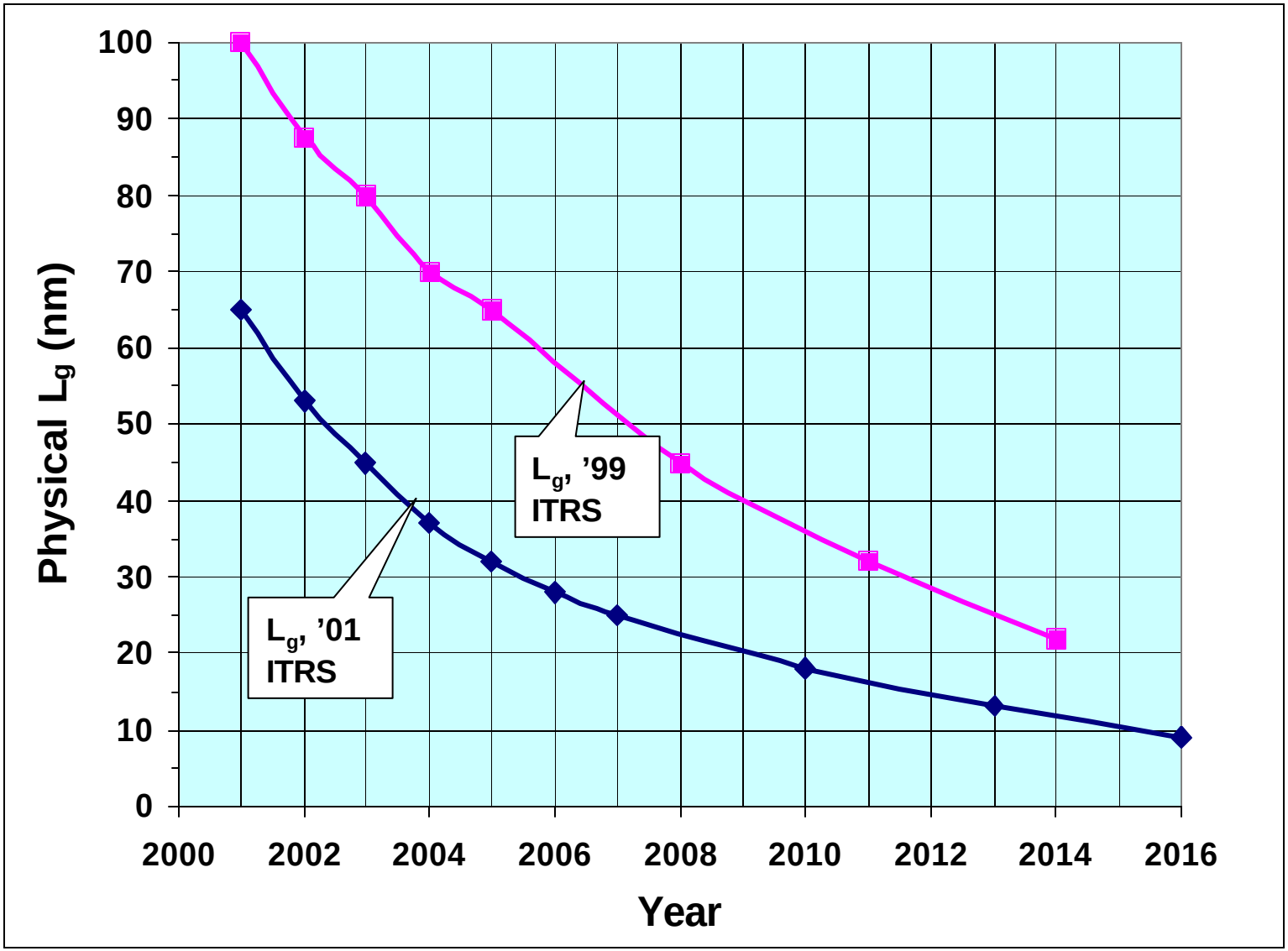
- Cost
- Power
- Speed
- Density
- Architecture
- Etc.

- V_{dd}
- Leakage
- Drive current
- Transistor size
- V_t control
- Etc.

- T_{ox}, L_g, S/D x_j
- Channel engineering
- High K gate dielec.
- Non-classical CMOS Structures
- Etc.

- Thermal processing
- Overall process flow
- Material properties
- Boron penetration
- Reliability
- Etc.

Accelerated L_g Scaling in 2001 ITRS



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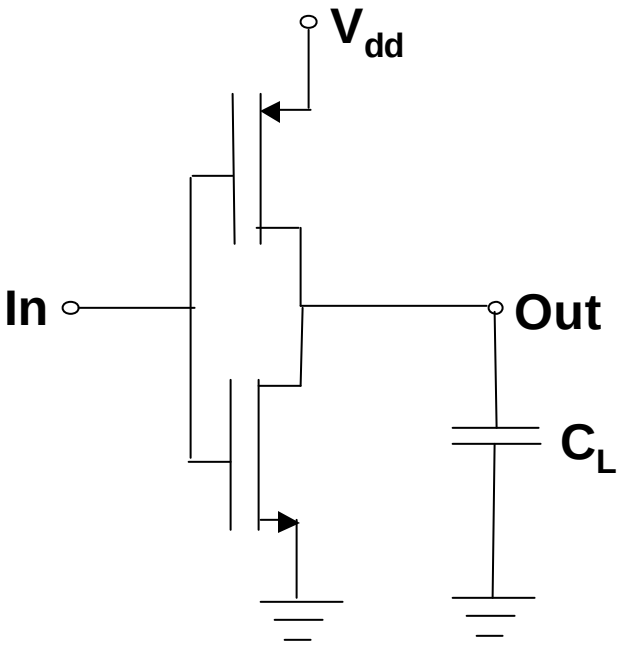
Key Metric for Transistor Speed

- Transistor intrinsic delay, τ
  - $\tau \sim C\ V_{dd}/(I_{on}*W)$
    - $C = C_{s/d} + C_L$
- Transistor intrinsic switching frequency = $1/\tau$: key performance metric
  - **To maximize 1/t, keep I_{on} high**



TRS Drivers for Different Applications

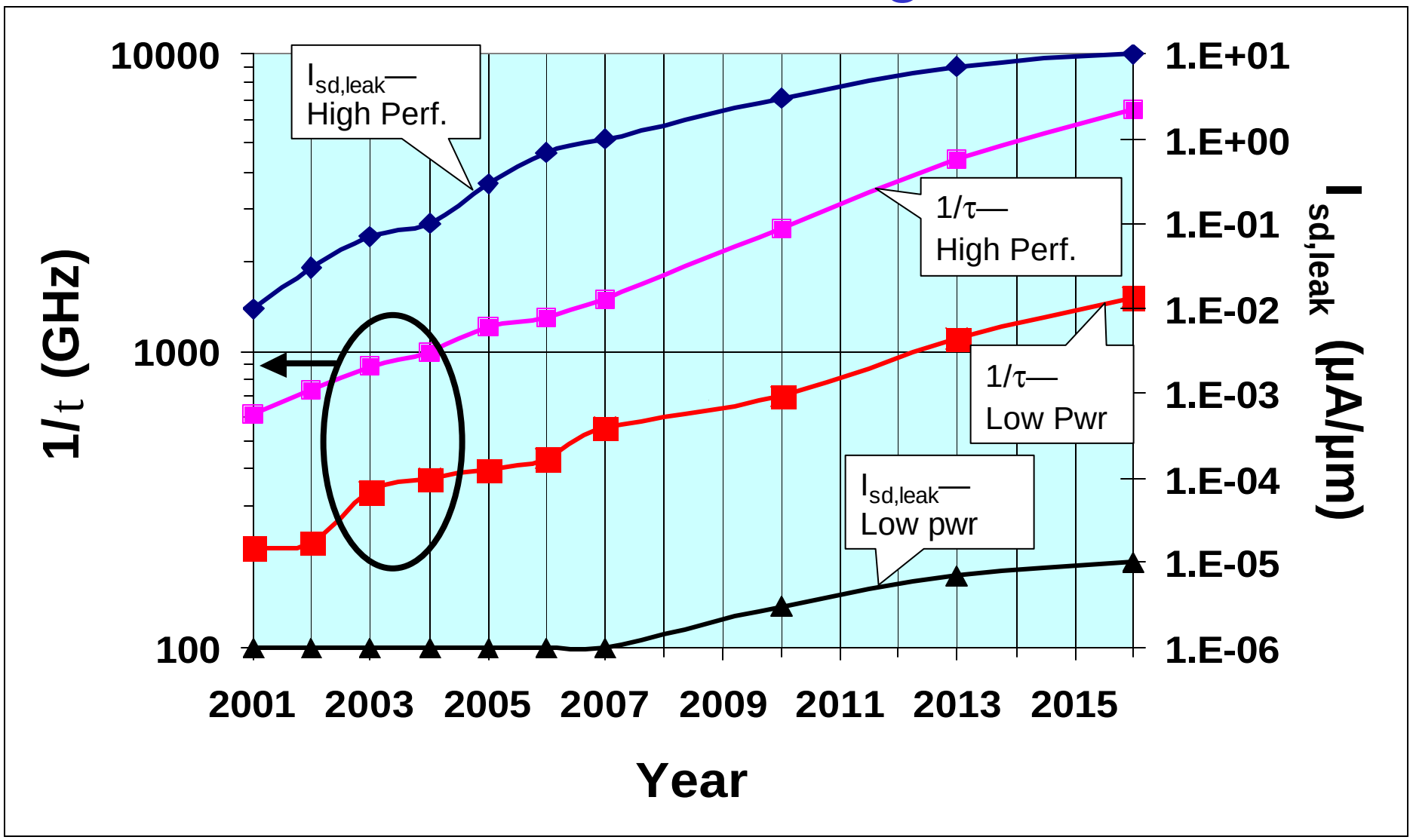
High performance chips (MPU, for example)

- **Driver: maximize chip speed→maximize transistor speed**
  - **Goal of ITRS scaling: 1/t increasing at ~ 17% per year, historical rate**
    - **Must keep I_{on} high**
    - **Consequently, I_{leak} is relatively high**

Low power chips (mobile applications)

- **Driver: minimize chip power→minimize I_{leak}**
  - **Goal of ITRS scaling: specific, low level of I_{leak}**
  - **Consequently, transistor performance is relatively reduced**

2001 ITRS Projections of 1/t and $I_{sd,leak}$ for High Performance and Low Power Logic



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Device Roadmap

arameter	Type	99	00	01	02	03	04	05	06	07	10	13	16
Tox (nm)	MPU	3.00	2.30	2.20	2.20	2.00	1.80	1.70	1.70	1.30	1.10	1.00	0.90
	LOP	3.20	3.00	2.2	2.0	1.8	1.6	1.4	1.3	1.2	1.0	0.9	0.8
	LSTP	3.20	3.00	2.6	2.4	2.2	2.0	1.8	1.6	1.4	1.1	1.0	0.9
Vdd	MPU	1.5	1.3	1.2	1.1	1.0	1.0	0.9	0.9	0.7	0.6	0.5	0.4
	LOP	1.3	1.2	1.2	1.2	1.1	1.1	1.0	1.0	0.9	0.8	0.7	0.6
	LSTP	1.3	1.2	1.2	1.2	1.2	1.2	1.2	1.2	1.1	1.0	0.9	0.9
Vth (V)	MPU	0.21	0.19	0.19	0.15	0.13	0.12	0.09	0.06	0.05	0.021	0.003	0.003
	LOP	0.34	0.34	0.34	0.35	0.36	0.32	0.33	0.34	0.29	0.29	0.25	0.22
	LSTP	0.51	0.51	0.51	0.52	0.53	0.53	0.54	0.55	0.52	0.49	0.45	0.45
Ion (uA/um)	MPU	1041	1022	926	959	967	954	924	960	1091	1250	1492	1507
	LOP	636	591	600	600	600	600	600	600	700	700	800	900
	LSTP	300	300	300	300	400	400	400	400	500	500	600	800
CV/I (ps)	MPU	2.00	1.64	1.63	1.34	1.16	0.99	0.86	0.79	0.66	0.39	0.23	0.16
	LOP	3.50	2.87	2.55	2.45	2.02	1.84	1.58	1.41	1.14	0.85	0.56	0.35
	LSTP	4.21	3.46	4.61	4.41	2.96	2.68	2.51	2.32	1.81	1.43	0.91	0.57
Ioff (uA/um)	MPU	0.00	0.01	0.01	0.03	0.07	0.10	0.30	0.70	1.00	3	7	10
	LOP	1e-4	1e-4	1e-4	1e-4	1e-4	3e-4	3e-4	3e-4	7e-4	1e-3	3e-3	1e-2
	LSTP	1e-6	1e-6	1e-6	1e-6	1e-6	1e-6	1-6	1e-6	1-6	3e-6	7e-6	1e-5
Gate L (nm)	MPU	100	70	65	53	45	37	32	30	25	18	13	9
	L(*)P	110	100	90	80	65	53	45	37	32	22	16	11

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High Performance Device Challenges

High leakage currents → serious static power dissipation problems

- **Direct tunneling increases as T_{ox} is reduced**
- **Static power problem especially for 2007 and beyond (requires high-k)**
- **Approaches to dealing with static power dissipation**
- **Multiple transistors with different V_t, T_{ox} (to reduce leakage)**
  - **High performance transistors used only where needed**
- **Design/architecture power management**
  - **i.e, temporarily turning off inactive function blocks**

Dimensional control: (T_{ox}, x_j's, L_g) scaling very rapidly

- **High performance: high power dissipation due to high leakage**

Poly depletion in gate electrode

- **Potential solution: metal electrode**

Mobility/transconductance enhancement, S/D parasitic resistance, …

Limits of Scaling Planar, Bulk MOSFETs

- 65 nm generation (2007) and beyond: increased difficulty in meeting all device requirements with classical planar, bulk CMOS
  - Control leakage and sustain performance for very small devices
  - Difficulty with fabricating ultra-small devices
  - Impact of quantum effects and statistical variation

- Alternate device structures (non-classical CMOS) may be utilized
  - Ultra-thin body SOI
  - Double gate SOI, including FinFET
  - Vertical FETs
  - Cf. “Emerging Research Devices” Chapter of ITRS

Summary

- MOSFET device scaling is driven by overall chip power, performance, and density requirements
- Scaling of devices for High Performance applications driven by transistor performance requirements
  - Scaling of devices for Low Power applications driven by transistor leakage requirements
- Key issues include I_{on} vs. I_{leak} tradeoffs, gate leakage, and need for improved mobility
- Potential solutions include high K gate dielectric, metal electrodes, and eventually, non-classical CMOS devices
  - High K needed first for Low Power (mobile) chips in 2005
    - High Performance: high K likely to follow, in 2007 or beyond

ITRS-2001 Lithography

2001 Highlights

- Optical lithography will be extended to the 65 nm node
- The insertion of Next Generation Lithography (NGL) is approaching
- Massive investments in NGL development are required, which may affect timing of nodes
- NGL masks have some very different requirements from optical masks
  - NGL mask tables are now inserted into the ITRS

Lithography Requirements - Overview

Year of Production	*2001*	*2002*	*2003*	*2004*	*2005*	*2006*	*2007*
	130 nm	*115 nm*	*100 nm*	*90 nm*	*80 nm*	*70 nm*	*65 nm*
DRAM							
Half pitch (nm)	130	115	100	90	80	70	65
Contacts (nm)	150	130	115	100	90	80	70
Overlay (nm, mean + 3 sigma)	45	40	35	31	28	25	23
CD control for critical layers (nm, 3 sigma, post-etch, 15% of CD) litho contribution, only	15.9	14.1	12.2	11	9.8	8.6	8
MPU/ASIC							
Half pitch	150	130	107	90	80	70	65
Gate length (nm, in resist)	90	75	65	53	45	40	35
Gate length (nm, post-etch) (physical length)	65	53	45	37	32	28	25
Contacts (nm, in resist)	150	130	115	100	90	80	70
Gate CD control (nm, 3 sigma, post-etch, 10% of CD, litho only)	5.3	4.3	3.7	3.0	2.6	2.3	2.0

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Microprocessor Gate CDs

- CDs must (???) be controlled to between ± 10% of the ***final*** dimension.
  - Aggressive MPU gate shrinks are creating stringent requirements on metrology and process control.
    - CD control of 2 nm (3σ) will be required for the 65 nm node in 2007.

Difficult Challenges: Near Term

Five difficult challenges [3] 65 nm before 2007.	Summary of issues
Optical and post-optical mask fabrication	• Registration, CD control, defectivity, and 157 nm films; defect free multi-layer substrates or membranes. • Equipment infrastructure (writers, inspection, repair).
Cost control and return-on-investment (ROI)	• Achieving constant/improved ratio of tool cost to throughput over time. • Cost-effective masks. • Sufficient lifetimes for the technologies,
Process control	• Processes to control gate CDs to less than 2 nm (3 s) • Alignment and overlay control to < 23 nm overlay.
Resists for ArF and F_2	• Outgassing, LER, SEM induced CD changes, defects £ 32 nm.
CaF_2	• Yield, cost, quality.

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Optical mask requirements

Year	*2001*	*2004*		*2007*	
Node	*130nm*	*90nm*		*65nm*	
Magnification	4	4	5	4	5
Mask OPC feature size (nm) Opaque	180	106	133	70	88
Image placement (nm, multi-point)	27	19	24	14	17
CD uniformity (nm, 3 sigma)					
Isolated lines (MPU gates) Binary	7.4	4.2	5.3	2.5	3.1
Isolated lines (MPU gates) ALT	10.4	5.9	7.4	4	5
Contact/vias	8	5.3	6.7	3.2	4
Defect size (nm)	104	72	90	52	65
Blank Flatness (nm)	250	180	280	130	200
Attenuated PSM transmission uniformity (+/-% of target)	4	4	4	4	4
Alternating PSM phase uniformity (+/- degree)	2	2	2	1	1

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Difficult Challenges: Long Term

Five difficult challenges < 65 nm beyond 2007.	Summary of issues
Mask fabrication and process control	• Defect-free NGL masks. • Equipment infrastructure (writers, inspection, repair). • Mask process control methods.
Metrology and defect inspection	• Capability for critical dimensions down to 9 nm and metrology for overlay down to 9 nm, and patterned wafer defect inspection for defects < 32 nm.
Cost control and return on investment (ROI)	• Achieving constant/improved ratio of tool cost to throughput. • Development of cost-effective post-optical masks. • Achieving ROI for industry with sufficient lifetimes for the technologies.
Gate CD control improvements; process control; resist materials	• Processes to control gate CDs < 1 nm (3 sigma) with appropriate line-edge roughness. • Alignment and overlay control methods to < 9 nm overlay.
Tools for mass production	• Post optical exposure tools capable of meeting requirements of the Roadmap.

Potential Solutions Timetable

Node	Year	Potential solutions
130 nm	2001	248 nm + PSM 193 nm
90 nm	2004	193 nm + PSM 157 nm *IPL, PEL, PXL*
65 nm	2007	157 nm + PSM EUV, EPL, ML2 *IPL, PEL, PXL*
45 nm	2010	EUV, EPL, ML2 *IPL, PEL, PXL*
32 nm	2013	EUV, EPL, ML2 *IPL, PEL, PXL*
22 nm	2016	EUV, EPL Innovation *IPL, PEL, PXL*

EUV = extreme ultraviolet

EPL = electron projection lithography

ML2 = maskless lithography

IPL = ion projection lithography

PXL = proximity x-ray lithography

PEL = proximity electron lithography

Technologies shown in italics have only single region support

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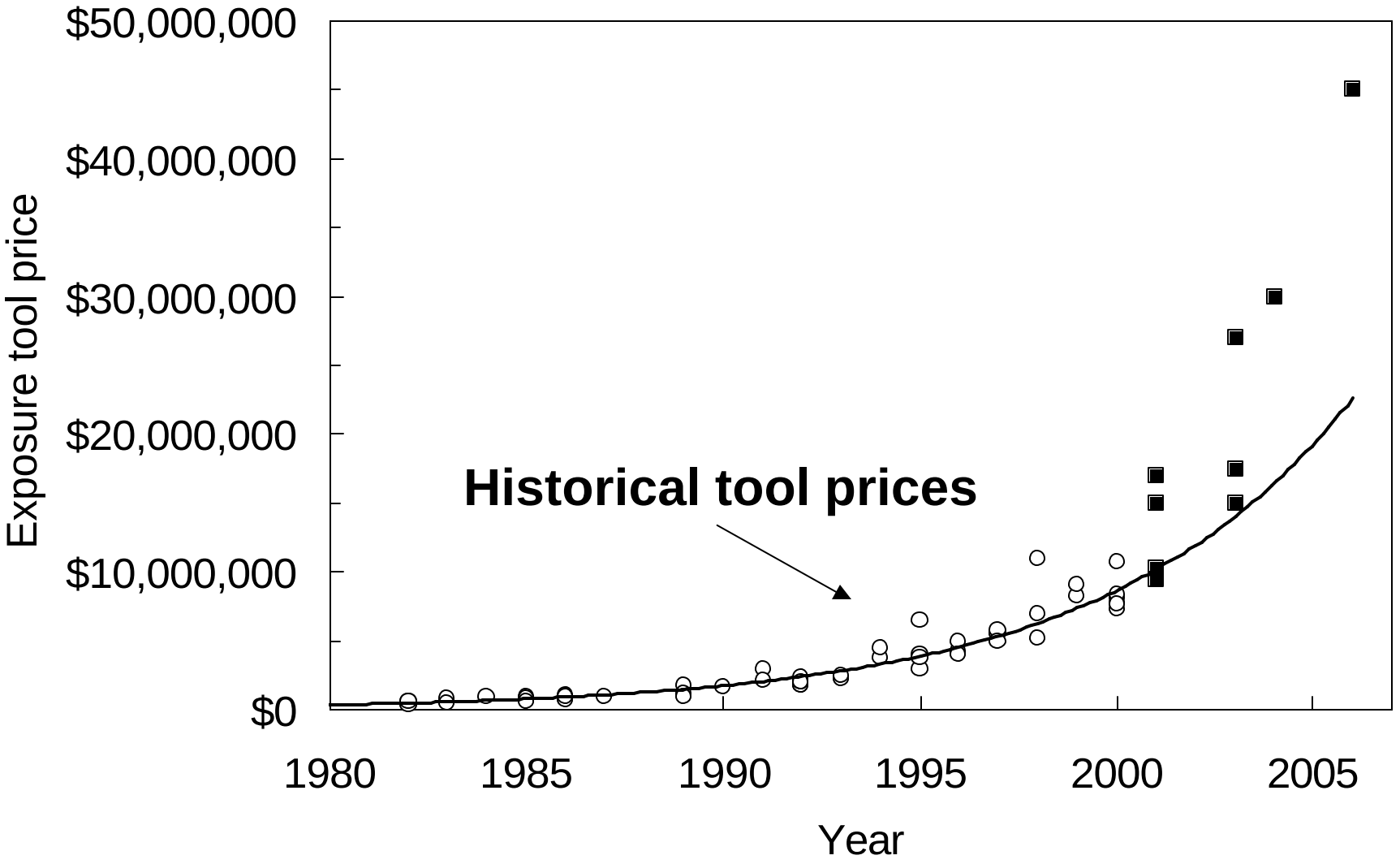
Lithography Costs



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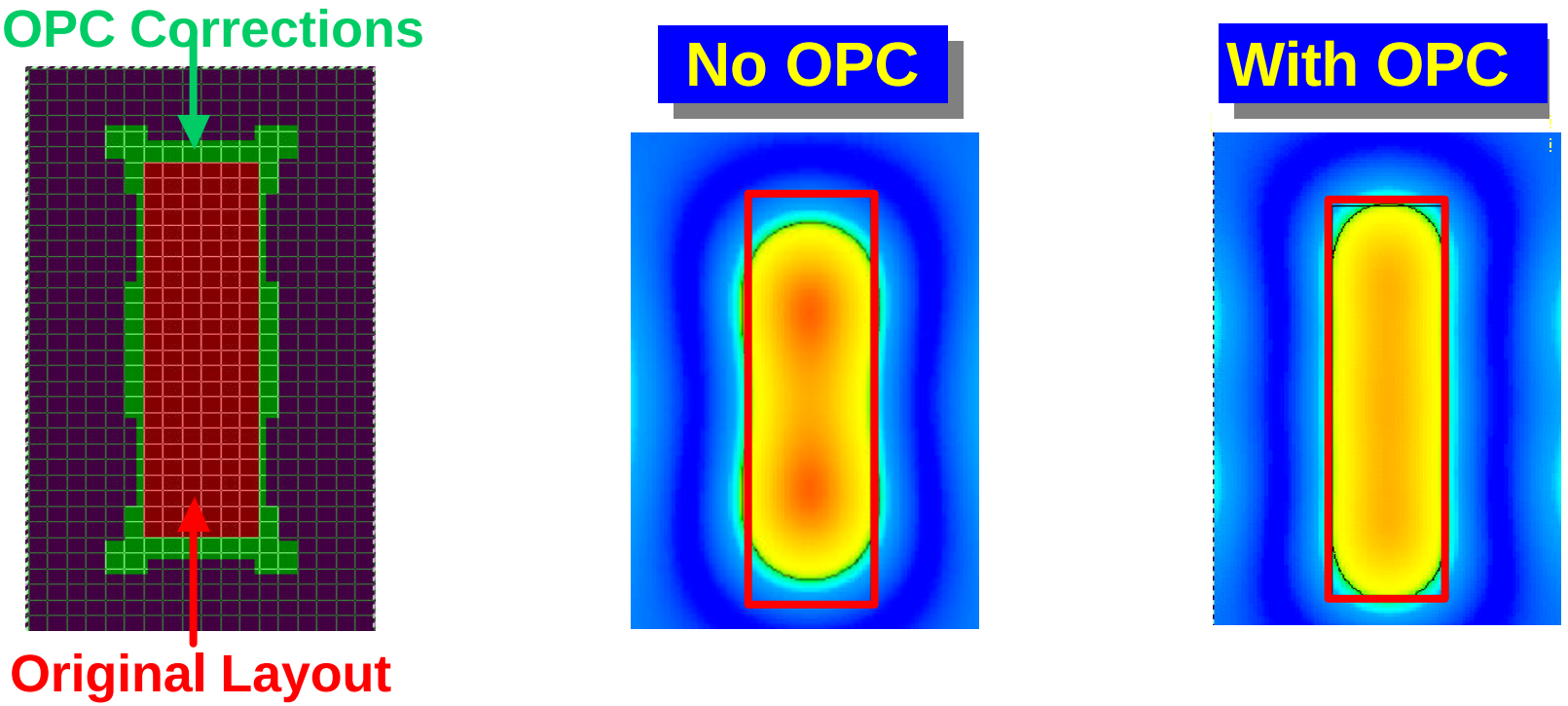
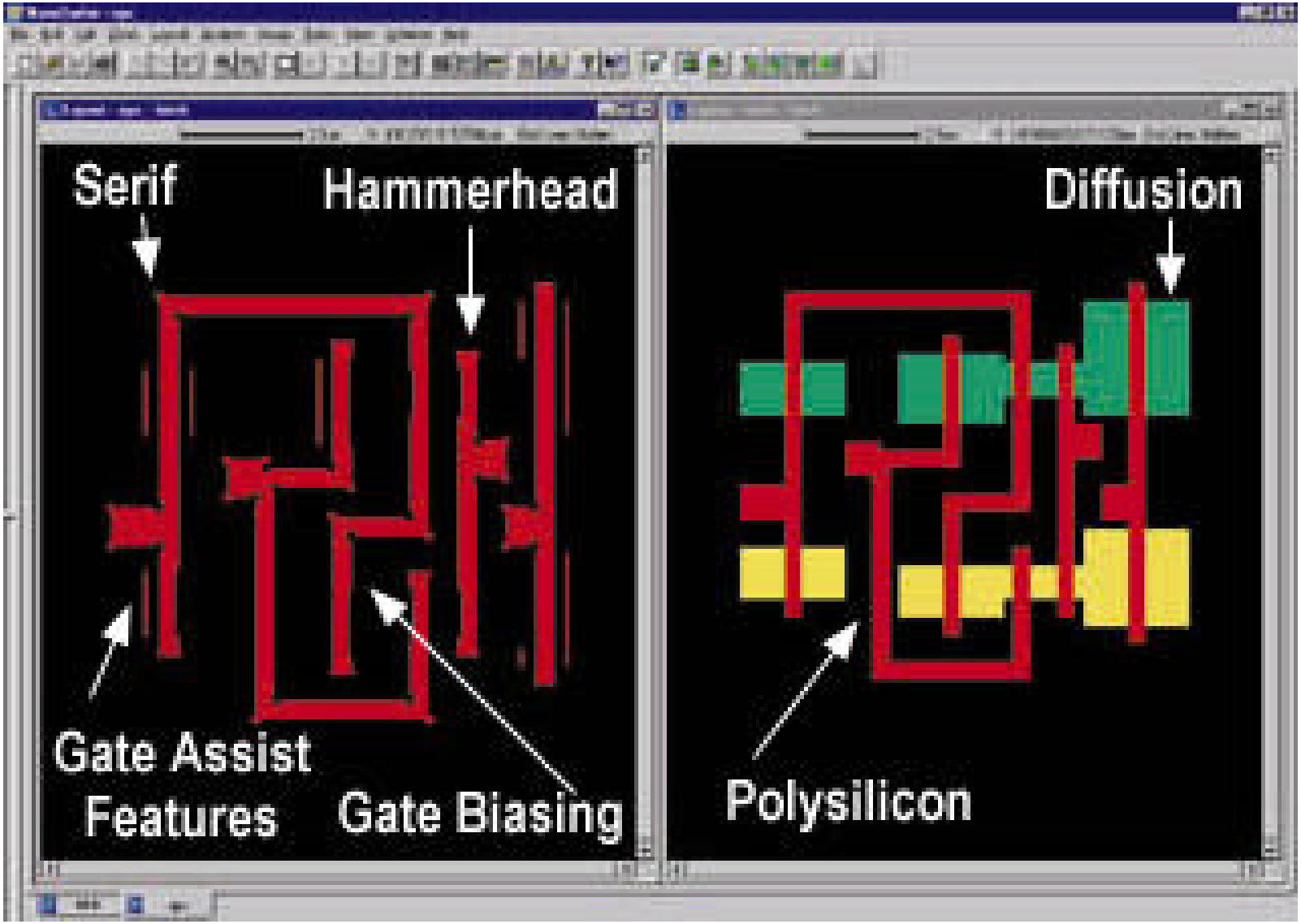
Optical Proximity Correction (OPC)

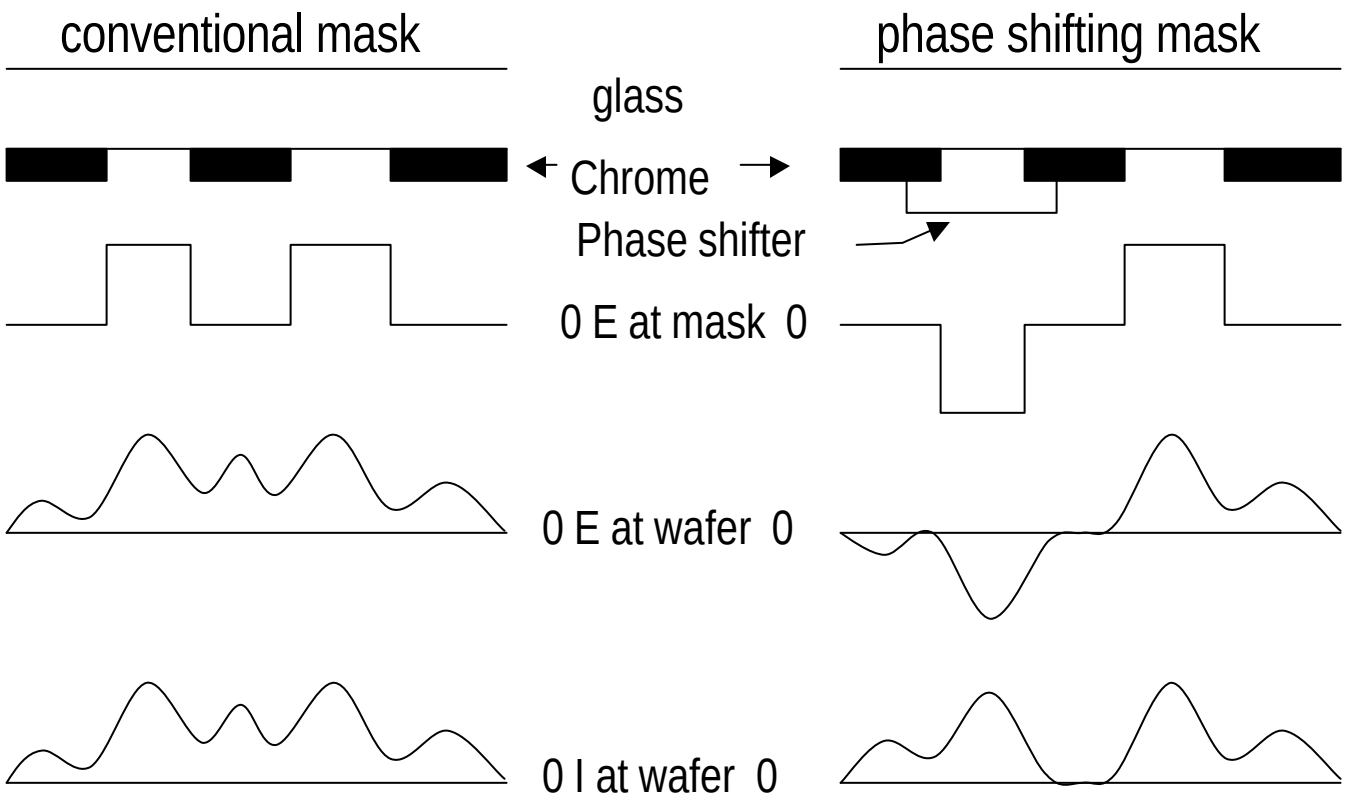
- Aperture changes to improve process control
  - improve yield (process window)
  - improve device performance



OPC Terminology



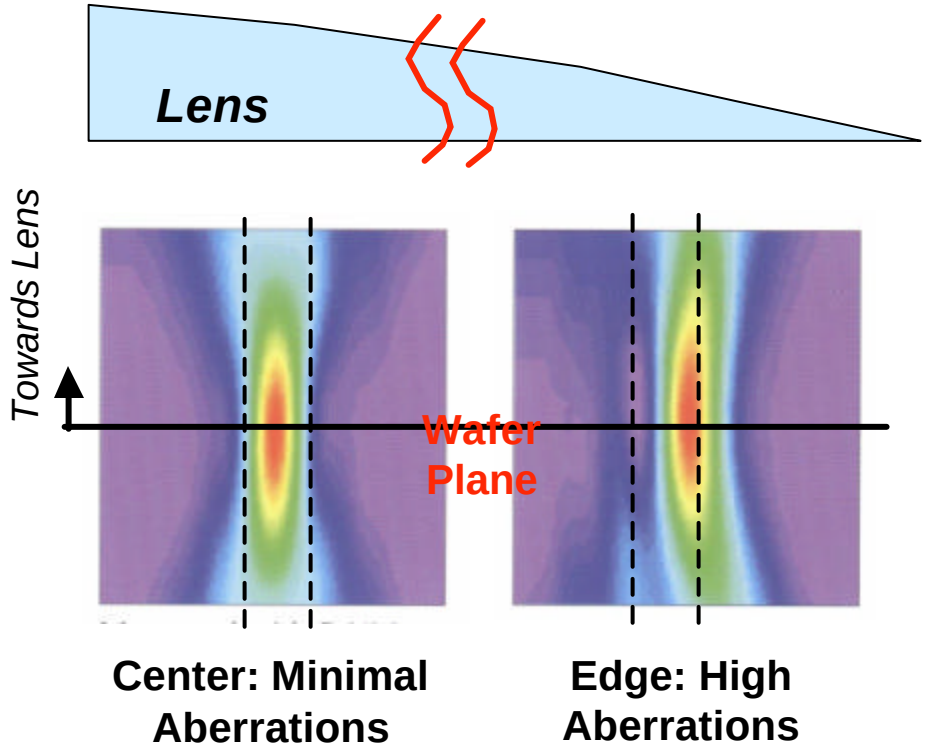
Phase Shifting Masks (PSM)

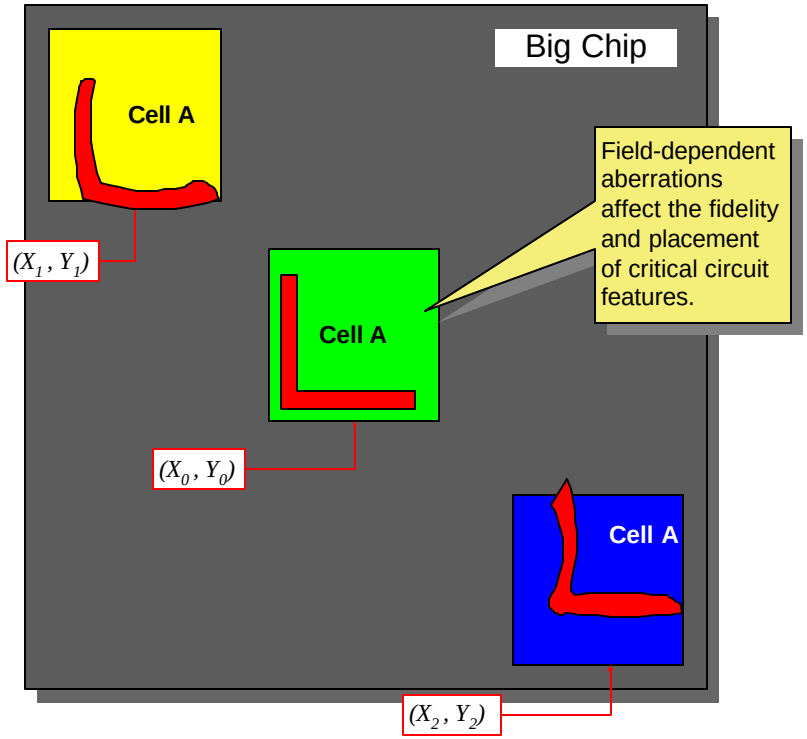


Many Other Optical Litho Issues

- Example: Field-dependent aberrations cause placement errors and distortions

$$\text{CELL\_A}(X_1, Y_1) \neq \text{CELL\_A}(X_0, Y_0) \neq \text{CELL\_A}(X_2, Y_2)$$





R. Pack, Cadence

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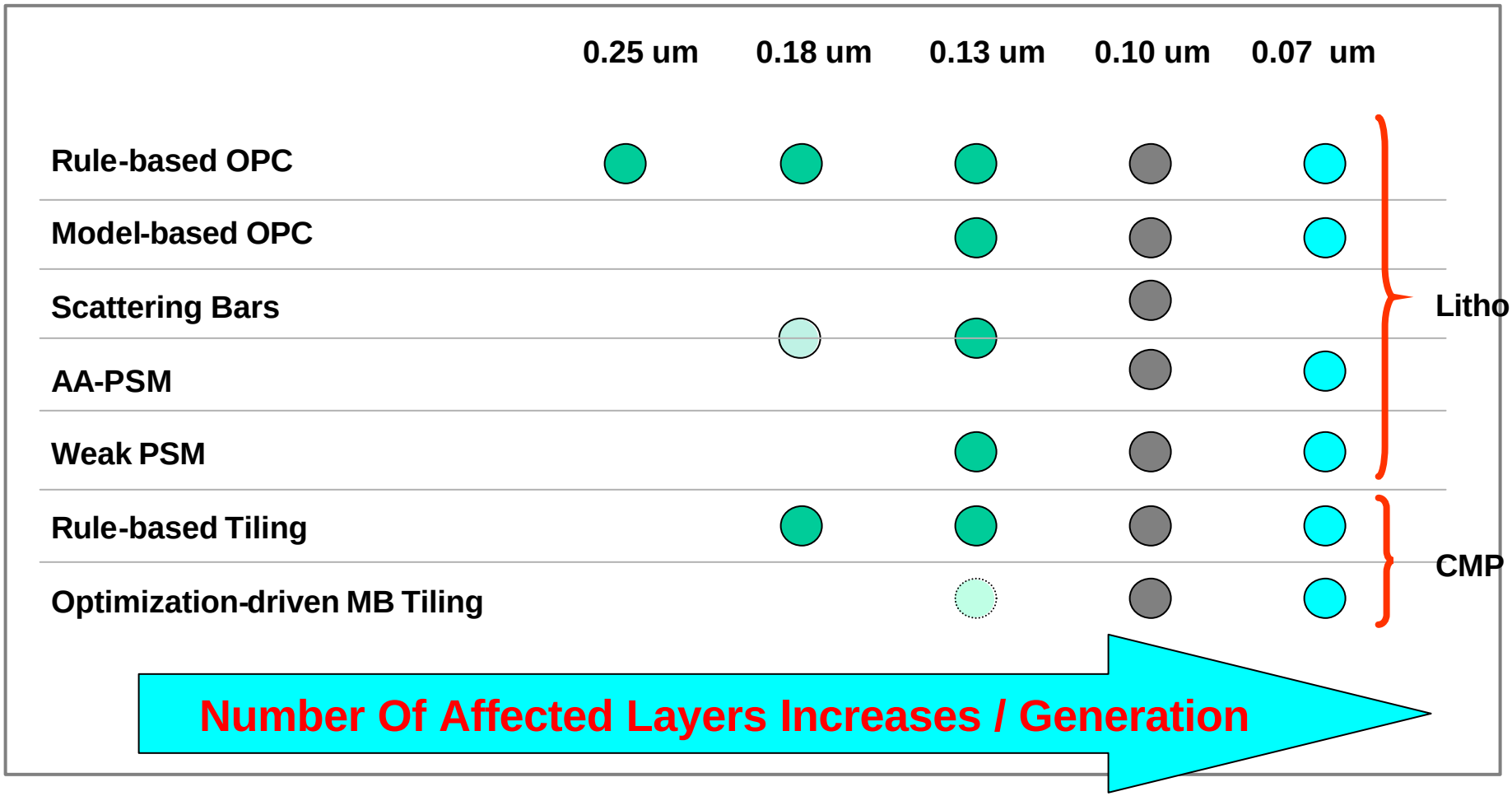
RET Roadmap



W. Grobman, Motorola – DAC-2001

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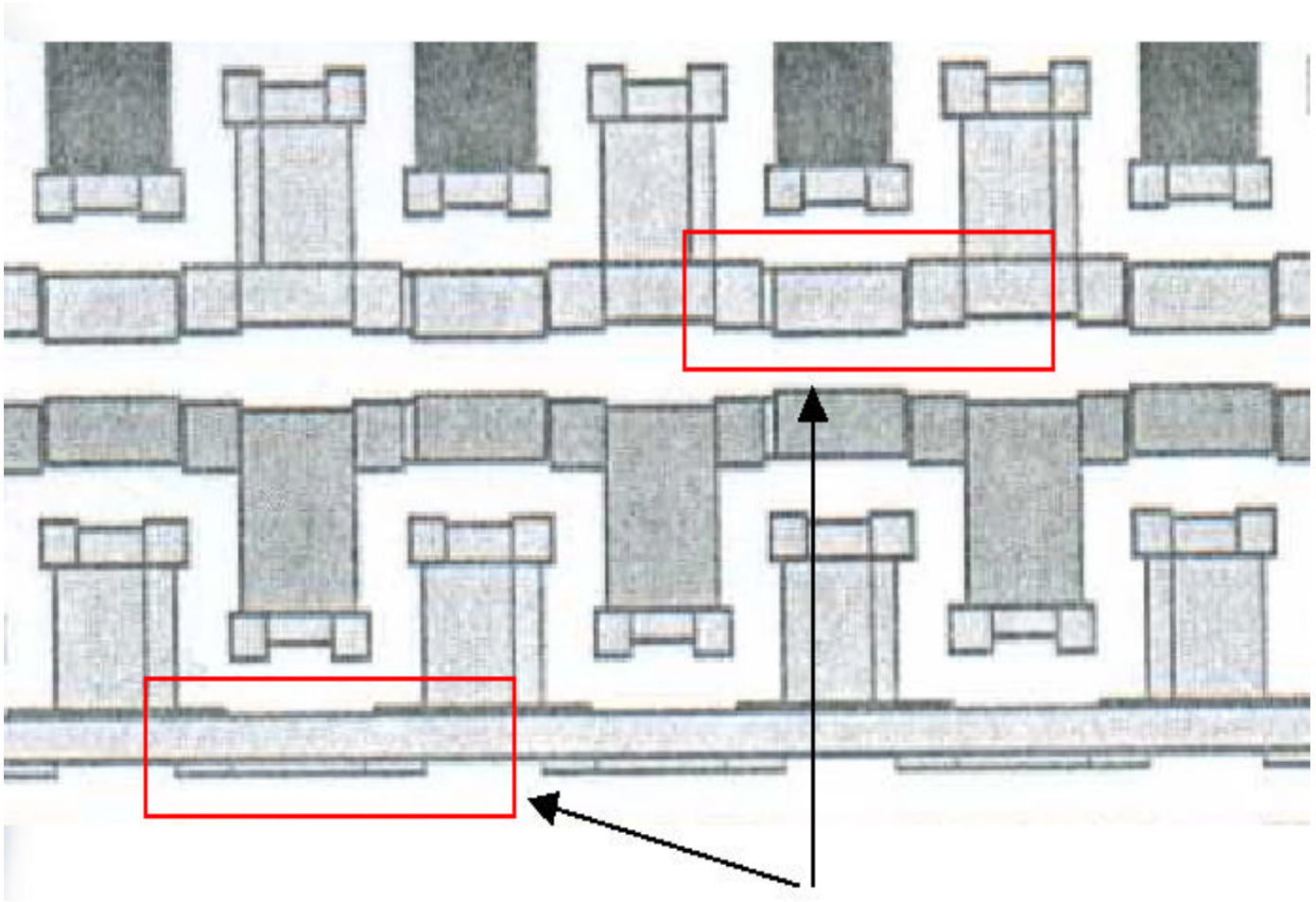
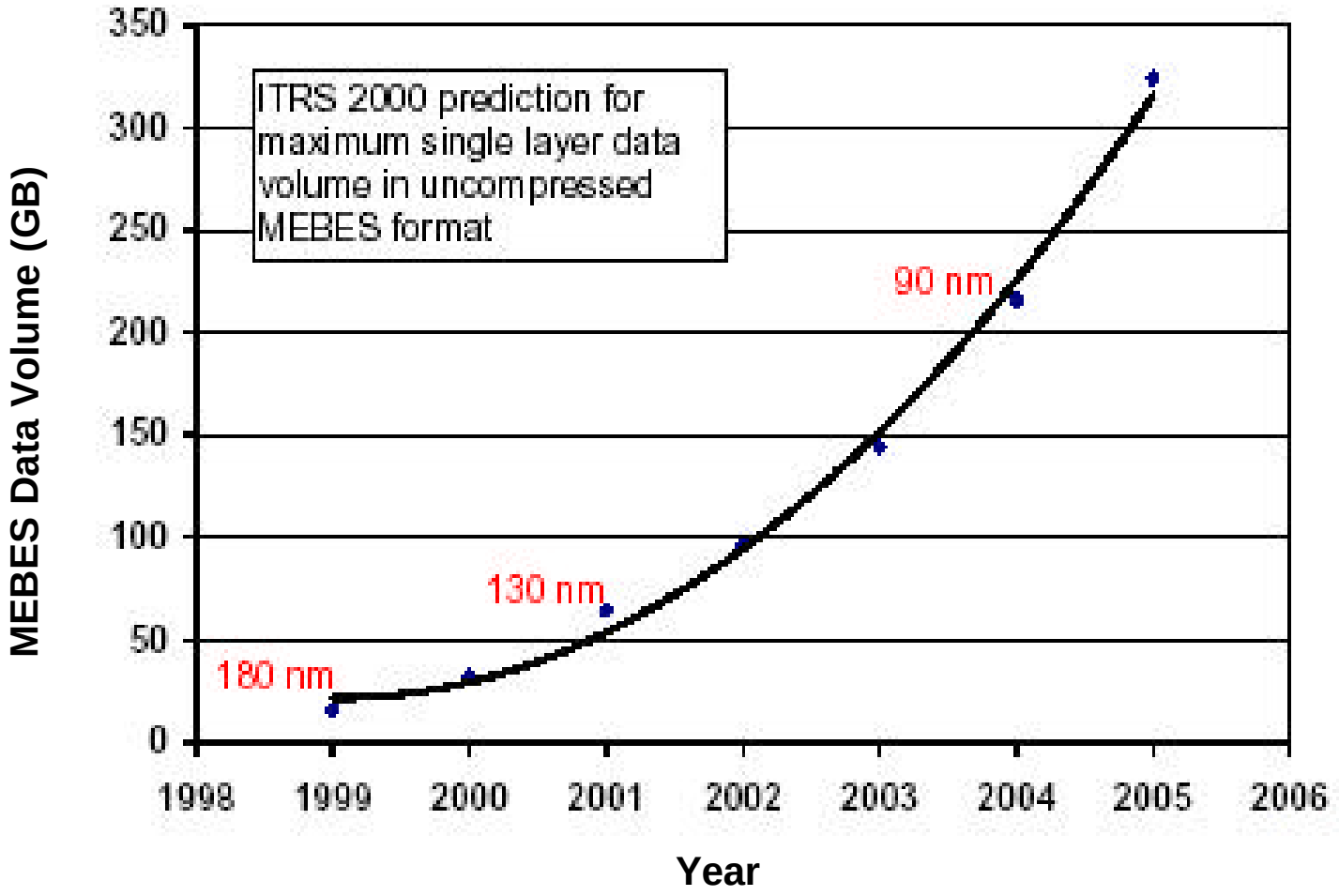
Context-Dependent Fracturing

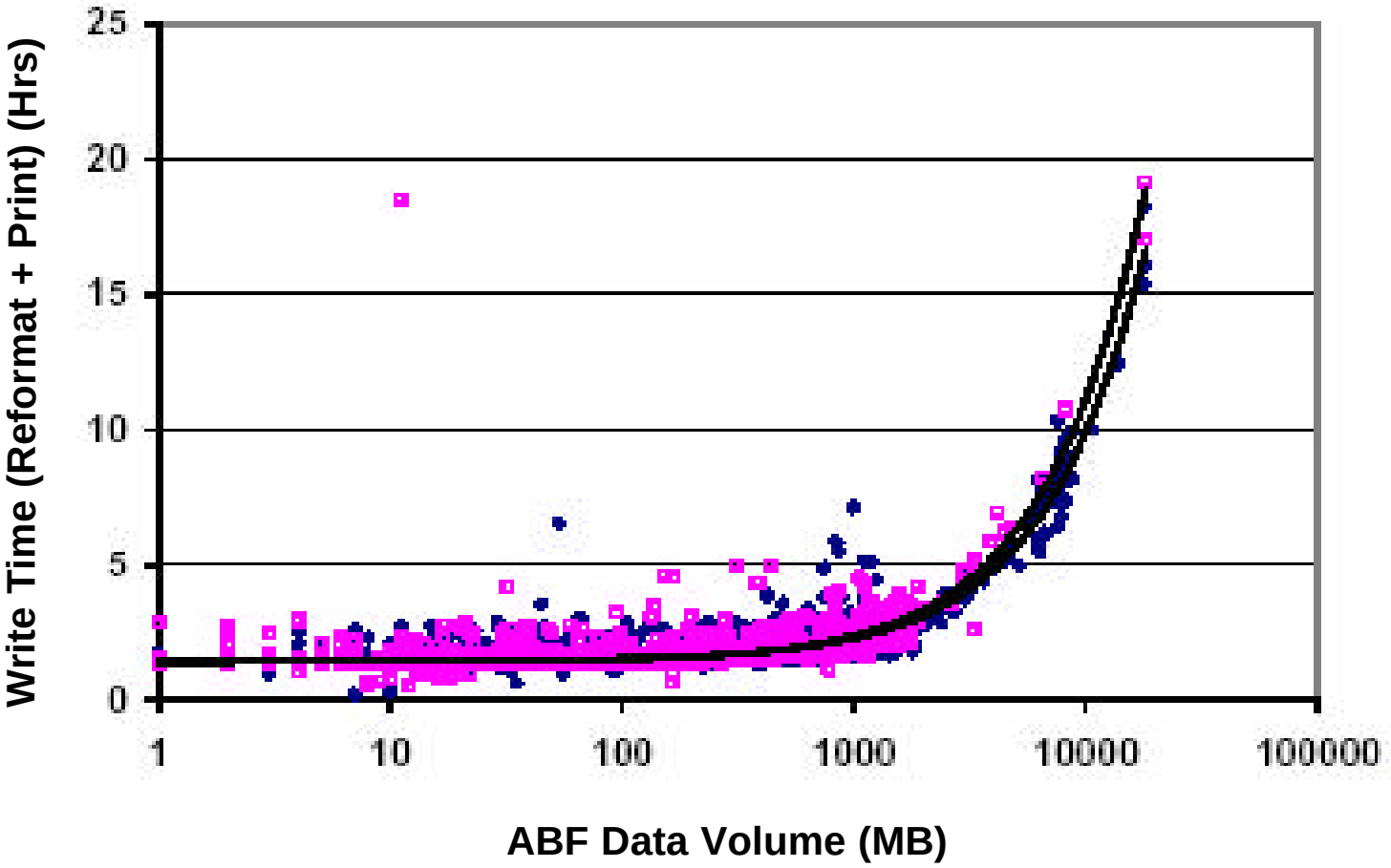


Same pattern, different fracture

ITRS Maximum Single Layer File Size



ALTA-3500 Mask Write Time



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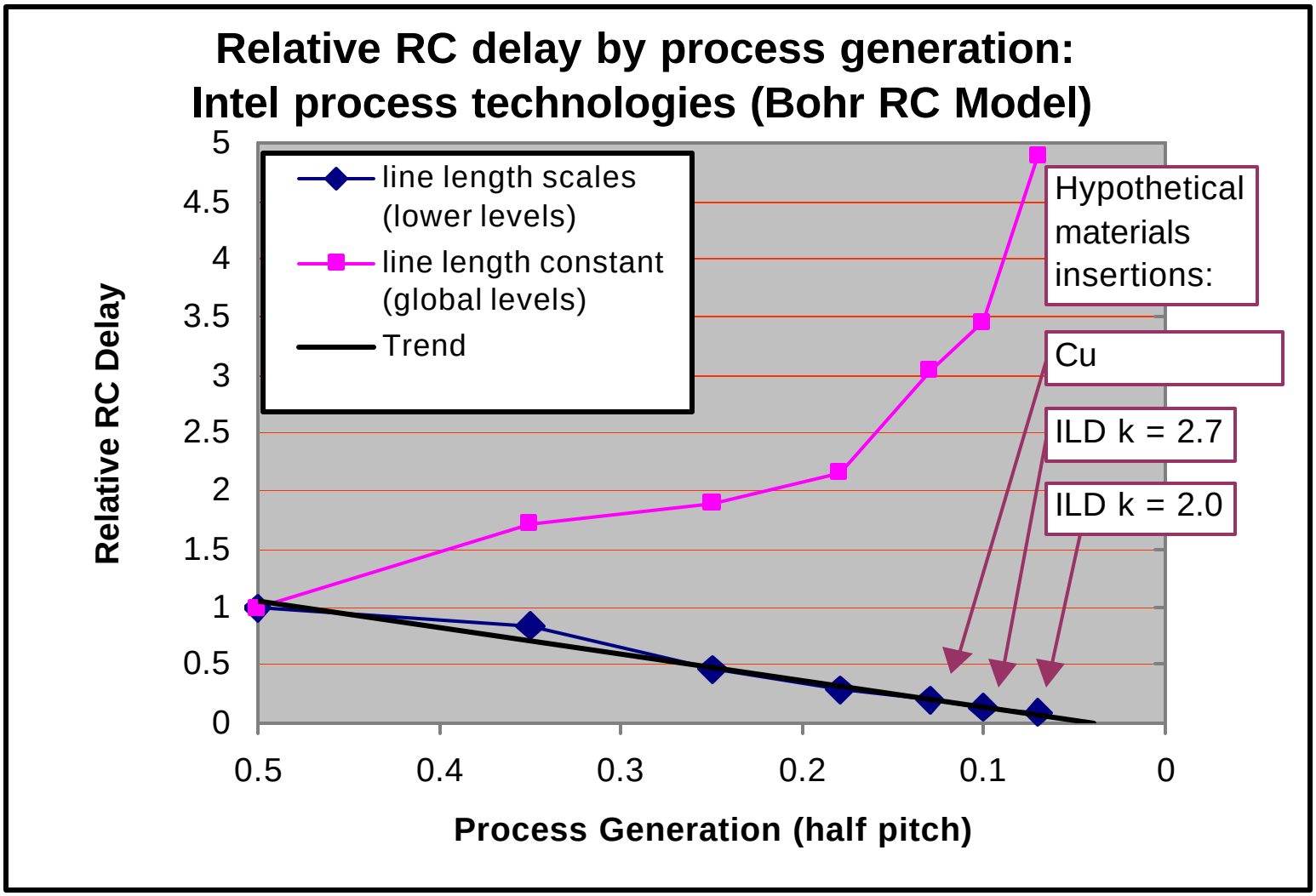
Summary – Causes of Major Changes

- Pushing optical lithography to its limits
  - Requires very tight mask CD control
- Introduction of next generation lithography (NGL)
  - Requires a new infrastructure
- Very aggressive gate shrinks
  - Dimensions less than 100 nm drive new requirements
- Need to contain lithography costs

ITRS-2001 Interconnect

No Moore Scaling!



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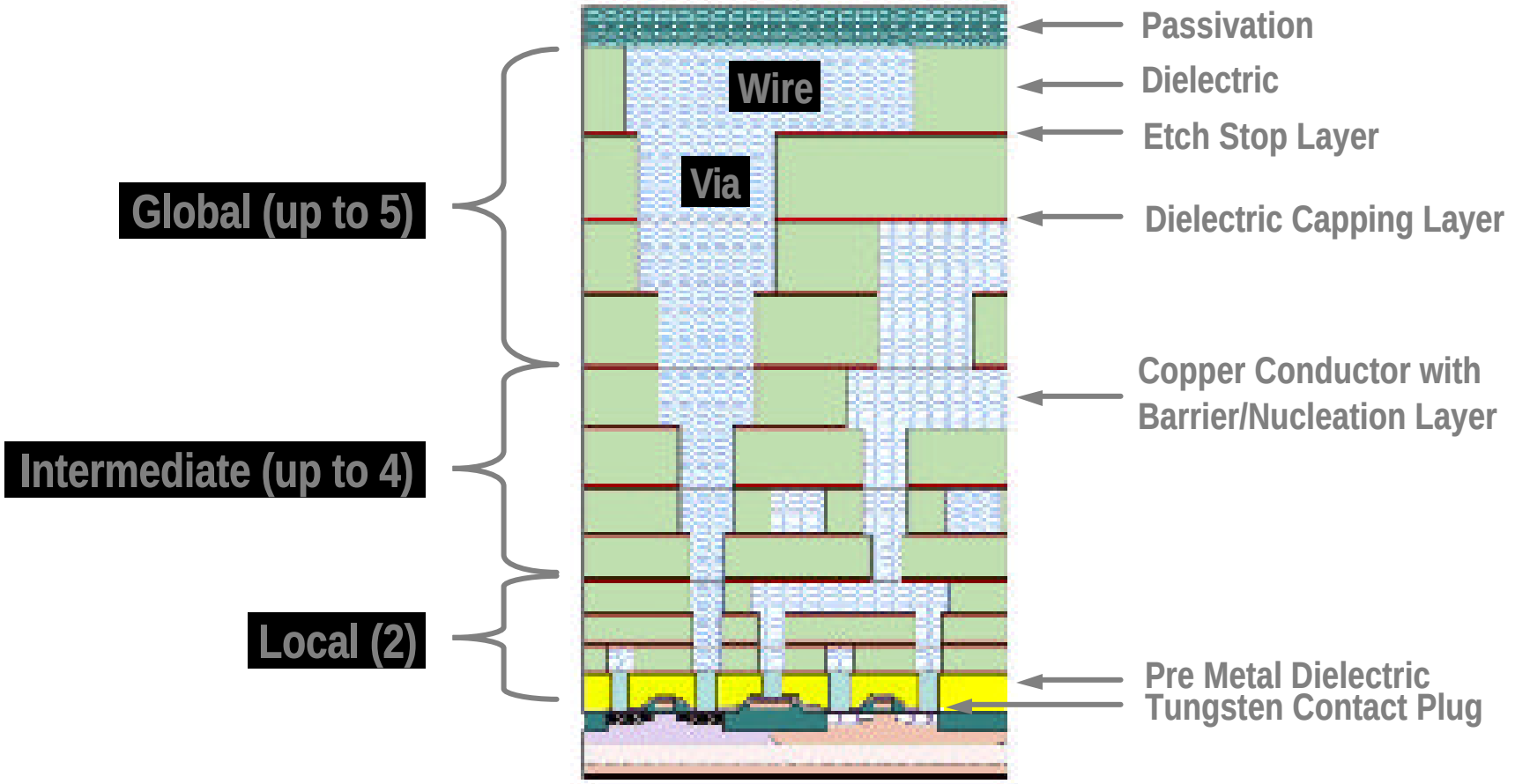
Typical chip cross-section illustrating hierarchical scaling methodology



Difficult Challenges

>65 nm

Introduction of new materials*

Integration of new processes and structures*

Achieving necessary reliability

Attaining dimensional control

Manufacturability and defect management that meet overall cost/performance requirements

<65 nm

- Dimensional control and metrology
- Patterning, cleaning and filling high aspect ratios features
- Integration of new processes and structures
- Continued introductions of new materials and size effects
- **Identify solutions which address global wiring scaling issues***

*** Top three grand challenges**

Dimensional Control

- 3D CD of features (e.g., dishing, erosion of copper)
  - performance and reliability implications
- Multiple levels
  - reduced feature size, new materials and pattern dependent processes
  - process interactions
    - CMP and deposition - dishing/erosion - thinning
    - Deposition and etch - to pattern multi-layer dielectrics
- Aspect ratios for etch and fill
  - particularly DRAM contacts and dual damascene

Technology Requirement Issues

- Wiring levels including “optional levels”
- Reliability metrics
- Wiring/via pitches by level
- Planarization requirements
- Conductor resistivity
- Barrier thickness
- Dielectric metrics including effective κ

Solutions beyond Cu and low k

- Material innovation combined with traditional scaling will no longer satisfy performance requirements
  - Design, packaging and interconnect innovation needed
  - Alternate conductors
    - optical, RF, low temperature
  - Novel active devices (3D or multi-level) in the interconnect

ITRS-2001 Assembly & Packaging

Market Sectors – From NEMI Roadmap

- Low cost - <$300 consumer products
- Hand held - <$1000 battery powered
- Cost performance <$3000 notebooks, desktop
- High performance >$3000 workstations, servers, network switches
- Harsh - Under the hood, and other hostile environments
- Memory - Flash, DRAM, SRAM
- A&P essentially the ONLY cost-driven chapter of ITRS

Difficult Challenges Near Term

- **Tools and methodologies to address chip and package co-design**
  - Mixed signal co-design and simulation (SI, Power, EMI)
  - For transient and localized hot spots - simulation of thermal mechanical stresses, thermal performance and current density in solder bumps
- **Improved Organic substrates**
  - Increased wireability and dimensional control at low cost
  - Higher temperature stability, lower moisture absorption, higher frequency capability
- **Improved (or elimination of) underfills for flip chip**
  - Improved underfill integration, adhesion, faster cure, higher temperature
- **Impact of Cu/low k on Packaging**
  - Direct wire bond and UBM/bump to Cu to reduce cost
  - Lower strength in low k which creates a weaker mechanical structure
- **Pb free and green materials at low cost**
  - Technical approaches are well defined but cost is not in line with needs

Difficult Challenges Long Term

- **Package cost may greatly exceed die cost**
  - Present R&D investments do not address this effectively
- **System level view to integrate chip, package, and system design**
  - Design will be distributed across industry specialist
- **Small high frequency, high power density, high I/O density die**
- **Increasing gap between device, package and board wiring density**
  - Cost of high density package substrates will dominate product cost

Summary: New Requirements and Cross-Cuts

- **Requirements:**
  - **Cost per pin numbers have adjusted down across all segments**
    - No Known solutions for many out year targets
    - Cost targets still put the cost of packaging well above cost of die
  - **Pin counts have been adjusted down**
    - Pin counts still drive wiring density in packages very aggressively
    - Signal and reference ratios added to help clarify test and design requirements
  - **Power continues to increase in the high end and related frequency for I/O has been increased to include new communications requirements**
- **Cross-Cuts:**
  - **Modeling of thermal and mechanical issues at package and device level which impact interconnect, test, design, modeling groups**
    - Stress transfer from package to device level
    - Handling of lower strength low k dielectric structures
    - Materials properties are not available for many applications
    - Device performance skew due to temperature differences that are driven by package design and system applications
  - **Power and pin count trends for design and test**
    - Probe, contactors, handling to cover pin count, pitch, power and frequency
    - Pin count which increases with flat die size which drives rapid increase in I/O density
  - **Rapid increase in frequency for emerging high speed serial I/O**
    - Impacts design, test

ITRS-2001 Design Chapter

Silicon Complexity Challenges

- Silicon Complexity = impact of process scaling, new materials, new device/interconnect architectures
- Non-ideal scaling (leakage, power management, circuit/device innovation, current delivery)
- Coupled high-frequency devices and interconnects (signal integrity analysis and management)
- Manufacturing variability (library characterization, analog and digital circuit performance, error-tolerant design, layout reusability, static performance verification methodology/tools)
- Scaling of global interconnect performance (communication, synchronization)
- Decreased reliability (SEU, gate insulator tunneling and breakdown, joule heating and electromigration)
- Complexity of manufacturing handoff (reticle enhancement and mask writing/inspection flow, manufacturing NRE cost)

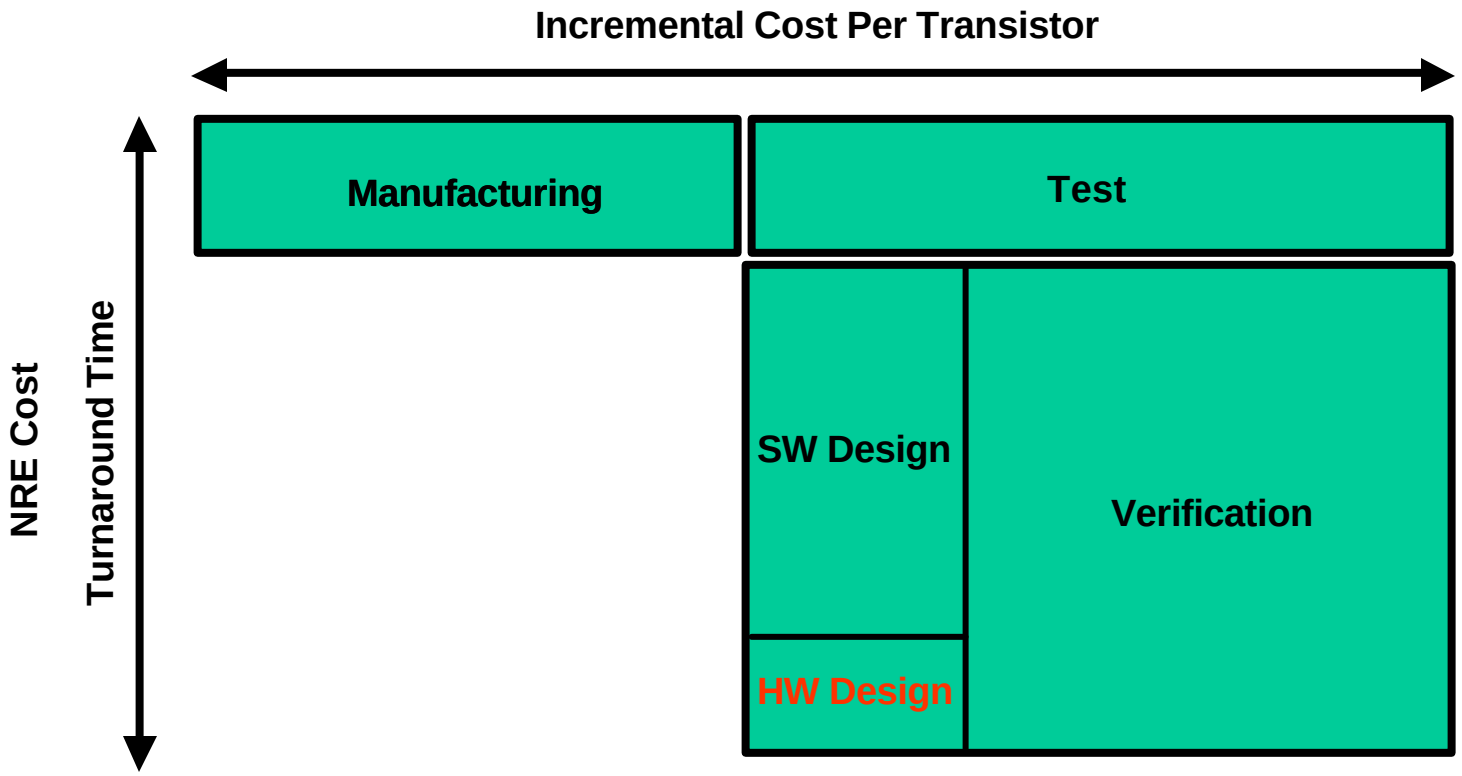
System Complexity Challenges

- System Complexity = exponentially increasing transistor counts, with increased diversity (mixed-signal SOC, …)
- Reuse (hierarchical design support, heterogeneous SOC integration, reuse of verification/test/IP)
- Verification and test (specification capture, design for verifiability, verification reuse, system-level and software verification, AMS self-test, noise-delay fault tests, test reuse)
- Cost-driven design optimization (manufacturing cost modeling and analysis, quality metrics, die-package co-optimization, …)
- Embedded software design (platform-based system design methodologies, software verification/analysis, codesign w/HW)
- Reliable implementation platforms (predictable chip implementation onto multiple fabrics, higher-level handoff)
- Design process management (team size / geog distribution, data mgmt, collaborative design, process improvement)

2001 Big Picture

- Message: Cost of Design threatens continuation of the semiconductor roadmap
  - New Design cost model
  - Challenges are now Crises
- Strengthen bridge between semiconductors and applications, software, architectures
  - Frequency and bits are not the same as efficiency and utility
  - New System Drivers chapter, with productivity and power foci
- Strengthen bridges between ITRS technologies
  - Are there synergies that “share red bricks” more cost-effectively than independent technological advances?
  - “Manufacturing Integration” cross-cutting challenge
  - “Living ITRS” framework to promote consistency validation

Design Technology Crises, 2001

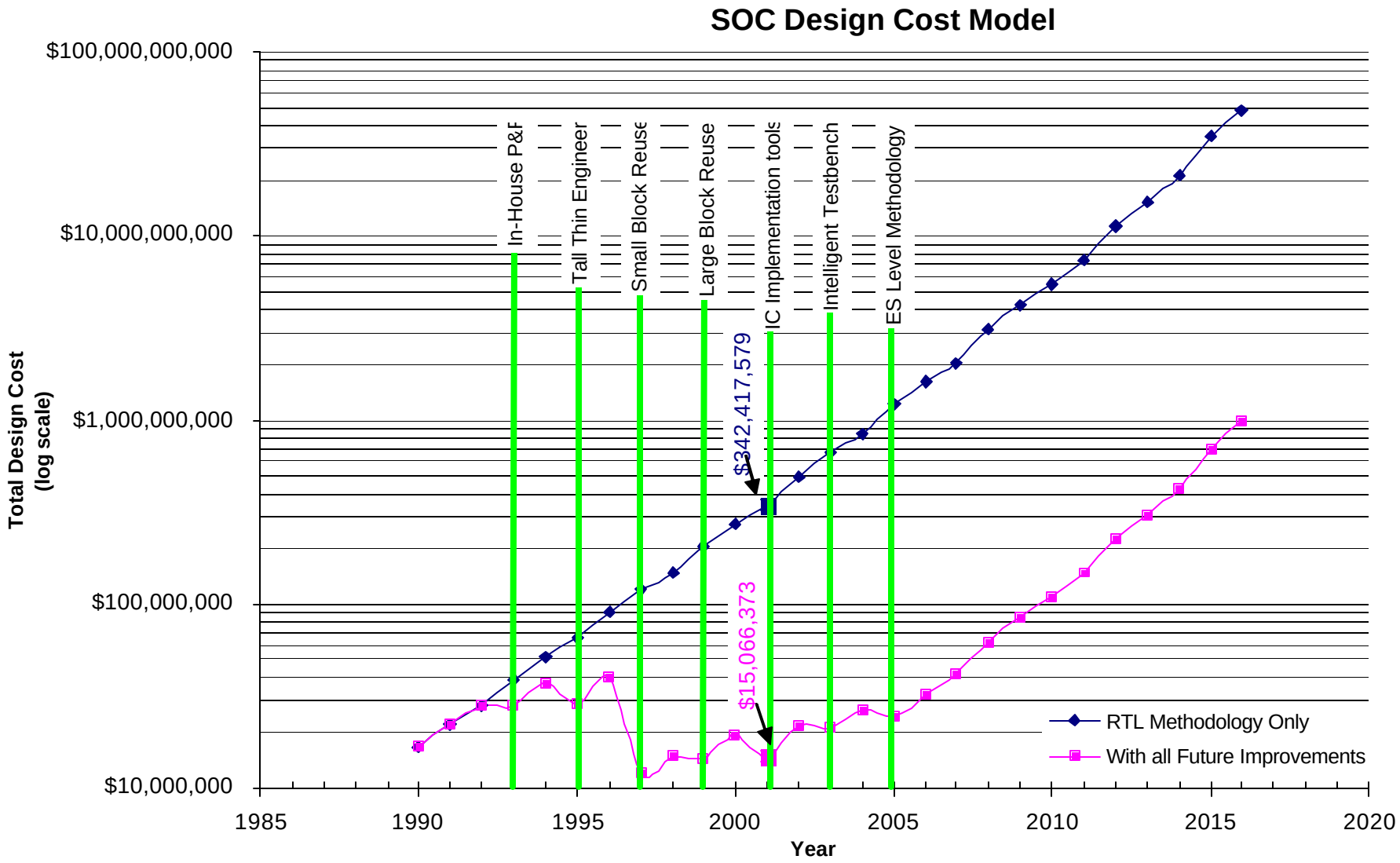


- 2-3X more verification engineers than designers on microprocessor teams
- Software = 80% of system development cost (and Analog design hasn't scaled
- Design NRE > 10's of $M ←→ manufacturing NRE $1M
- Design TAT = months or years ←→ manufacturing TAT = weeks
- Without DFT, test cost per transistor grows exponentially relative to mfg cost

Design Cost Model

- Engineer cost per year increases 5% / year ($181,568 in 1990)
- EDA tool cost per year (per engineer) increases 3.9% per year ($99,301 in 1990)
- Productivity due to 8 major Design Technology innovations (3.5 of which are still unavailable) : RTL methodology; In-house P&R; Tall-thin engineer; Small-block reuse; Large-block reuse; IC implementation suite; Intelligent testbench; Electronic System-level methodology
- Matched up against SOC-LP PDA content:
  - SOC-LP PDA design cost = $15M in 2001
  - Would have been $342M without EDA innovations and the resulting improvements in design productivity

Design Cost of SOC-LP PDA Driver



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Cross-Cutting Challenge: Productivity

- Overall design productivity of normalized functions on chip must scale at 4x per node for SOC Driver
- Reuse (including migration) of design, verification and test effort must scale at > 4x/node
- Analog and mixed-signal synthesis, verification and test
- Embedded software productivity

Cross-Cutting Challenge: Power

- Reliability and performance analysis impacts
- Accelerated lifetime testing (burn-in) paradigm fails
- Large power management gaps (standby power for low-power SOC; dynamic power for MPU)
- Power optimizations must *simultaneously* and *fully* exploit many degrees of freedom (multi-Vt, multi-Tox, multi-Vdd in core) while guiding architecture, OS and software

Cross-Cutting Challenge: Interference

- Lower noise headroom especially in low-power devices
- Coupled interconnects
- Supply voltage IR drop and ground bounce
- Thermal impact (e.g., on device off-currents and interconnect resistivities)
- Mutual inductance
- Substrate coupling
- Single-event (alpha particle) upset
- Increased use of dynamic logic families
- Modeling, analysis and estimation at all levels of design

Cross-Cutting Challenge: Error-Tolerance

- Relaxing 100% correctness requirement may reduce manufacturing, verification, test costs
- Both transient and permanent failures of signals, logic values, devices, interconnects
- Novel techniques: adaptive and self-correcting / self-repairing circuits, use of on-chip reconfigurability

2001 Big Picture = Big Opportunity

- Why ITRS has "red brick" problems
  - "Wrong" Moore's Law
    - Frequency and bits are not the same as efficiency and utility
    - No awareness of applications or architectures (only Design is aware)
  - Independent, "linear" technological advances don't work
    - Car has more drivers (mixed-signal, mobile, etc. applications)
    - Every car part thinks that it is the engine → too many red bricks
  - No clear ground rules
    - Is cost a consideration? Is the Roadmap only for planar CMOS?
- New in 2001: Everyone asks "Can Design help us?"
  - Process Integration, Devices & Structures (PIDS): 17%/year improvement in CV/I metric → sacrifice Ioff, Rds, …analog, LOP, LSTP, … many flavors
  - Assembly and Packaging: cost limits → keep bump pitches high → sacrifice IR drop, signal integrity (impacts Test as well)
  - Interconnect, Lithography, PIDS/Front-End Processes: What variability can Designers tolerate? 10%? 15%? 25%?

"Design-Manufacturing Integration"

- 2001 ITRS Design Chapter: "Manufacturing Integration" = one of five Cross-Cutting Challenges
- Goal: share red bricks with other ITRS technologies
  - Lithography CD variability requirement → new Design techniques that can better handle variability
  - Mask data volume requirement → solved by Design-Mfg interfaces and flows that pass functional requirements, verification knowledge to mask writing and inspection
  - ATE cost and speed red bricks → solved by DFT, BIST/BOST techniques for high-speed I/O, signal integrity, analog/MS
  - Does "X initiative" have as much impact as copper?

Example: Manufacturing Test

- High-speed interfaces (networking, memory I/O)
  - Frequencies on same scale as overall tester timing accuracy
- Heterogeneous SOC design
  - Test reuse
  - Integration of distinct test technologies within single device
  - Analog/mixed-signal test
- Reliability screens failing
  - Burn-in screening not practical with lower Vdd, higher power budgets → overkill impact on yield
- Design Challenges: DFT, BIST
  - Analog/mixed-signal
  - Signal integrity and advanced fault models
  - BIST for single-event upsets (in logic as well as memory)
  - Reliability-related fault tolerance

Example: Lithography

- 10% CD uniformity requirement causes red bricks
- 10% < 1 atomic monolayer at end of ITRS
- This year: Lithography, PIDS, FEP agreed to relax CD uniformity requirement (but we still see red bricks)
- Design challenge: Design for variability
  - Novel circuit topologies
  - Circuit optimization (conflict between slack minimization and guardbanding of quadratically increasing delay sensitivity)
  - Centering and design for $/wafer
- Design challenge: Design for when devices, interconnects no longer 100% guaranteed correct
  - Can this save $$$ in manufacturing, verification, test costs?

Example: Dielectric Permittivity

YEAR / *TECHNOLOGY NODE*	*2001*	*2002*	*2003*	*2004*	*2005*	*2006*	*2007*
DRAM ½ PITCH (nm) (SC. 2.0)	*130*	*115*	*100*	*90*	*80*	*70*	*65*
MPU/ASIC ½ PITCH (nm) (SC. 3.7)	*150*	*130*	*107*	*90*	*80*	*70*	*65*
MPU PRINTED GATE LENGTH (nm) (SC. 3.7)	*90*	*75*	*65*	*53*	*45*	*40*	*35*
MPU PHYSICAL GATE LENGTH (nm) (SC. 3.7)	*65*	*53*	*45*	*37*	*32*	*28*	*25*
Conductor effective resistivity (mW-cm) Cu intermediate wiring*	**2.2**	**2.2**	**2.2**	**2.2**	**2.2**	**2.2**	**2.2**
Barrier/cladding thickness (for Cu intermediate wiring) (nm)	**18**	**15**	**13**	**11**	**10**	**9**	**8**
Interlevel metal insulator —effective dielectric constant (k)	**3.0-3.7**	**3.0–3.7**	**2.9–3.5**	**2.5–3.0**	**2.5–3.0**	**2.5–3.0**	**2.0–2.5**
Interlevel metal insulator (minimum expected) —bulk dielectric constant (k)	**2.7**	**2.7**	**2.7**	**2.2**	**2.2**	**2.2**	**1.7**

Bulk and effective dielectric constants

Porous low-k requires alternative planarization solutions

Cu at all nodes - conformal barriers

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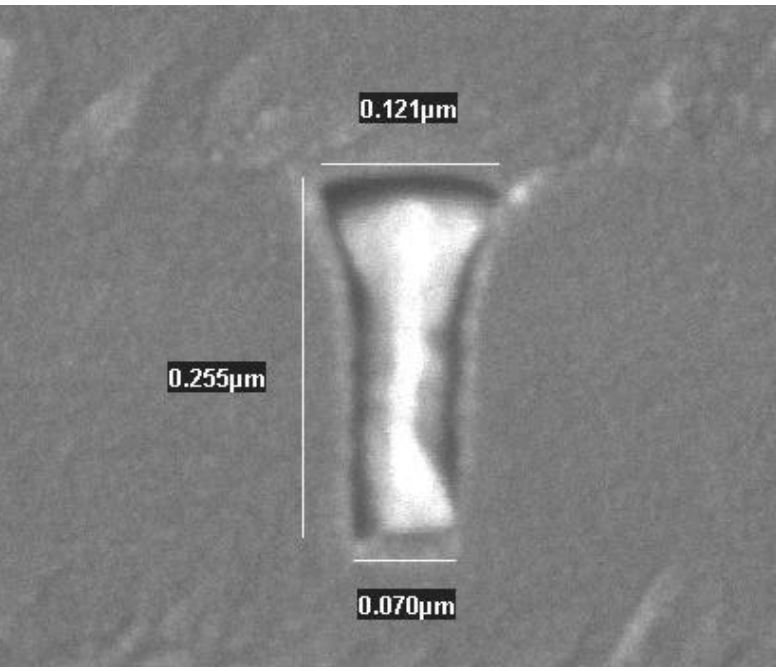
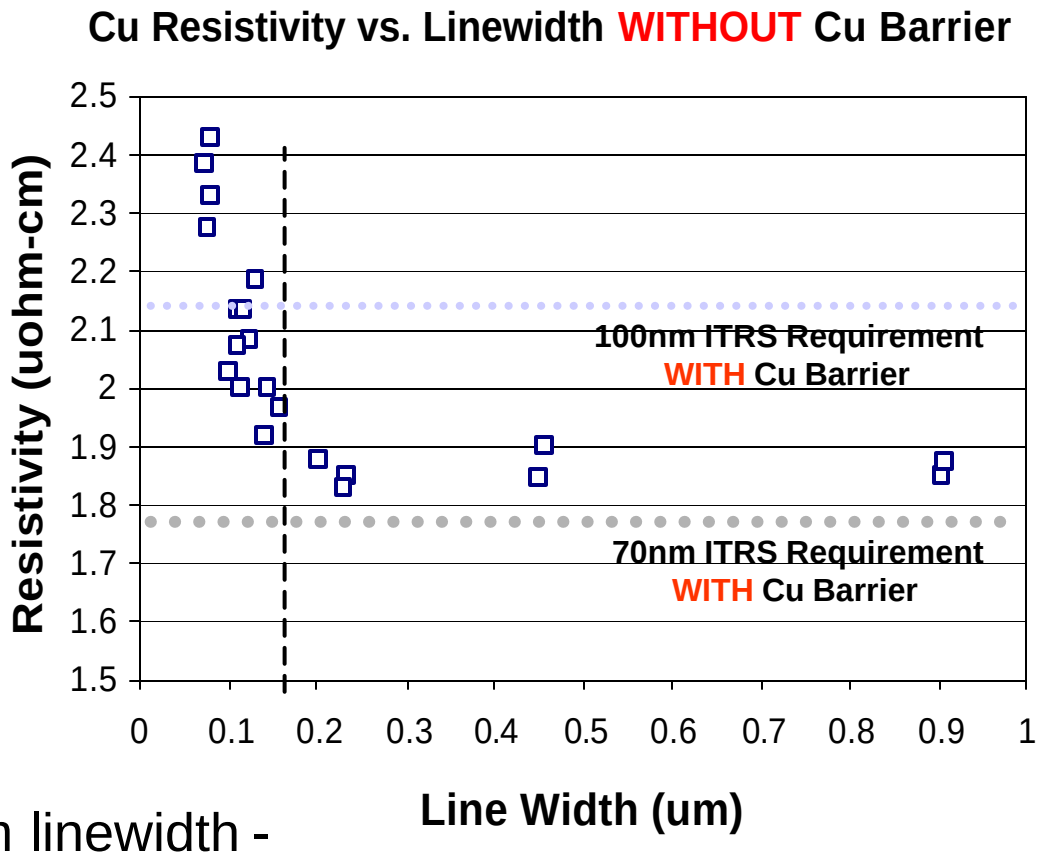
Will Copper Continue To Be Worth It?





Conductor resistivity increases
expected to appear around 100 nm linewidth -
will impact intermediate wiring first - ~ 2006

Courtesy of SEMATECH

C. Case, BOC Edwards – ITRS-2001 preliminary

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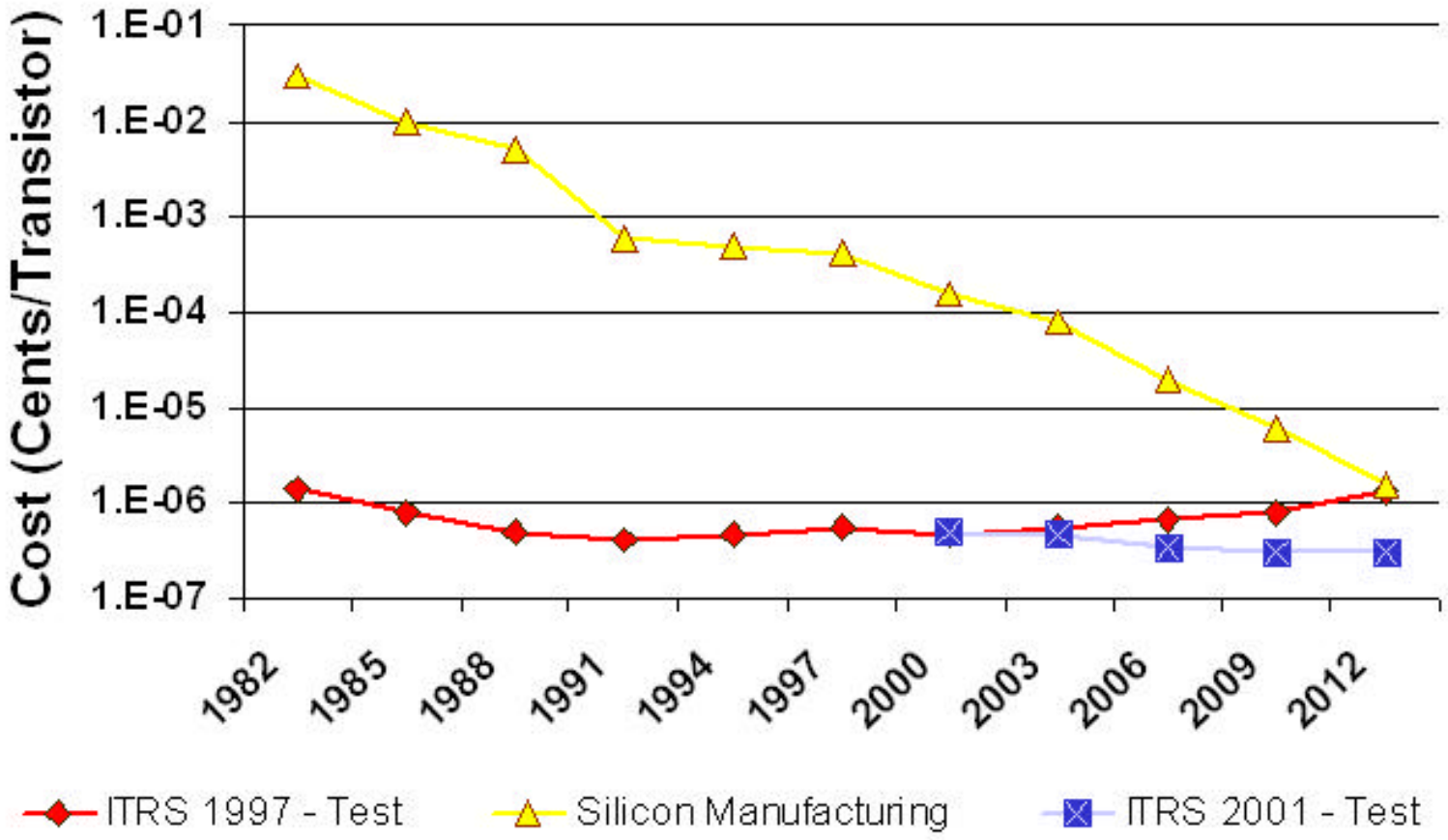
Cost of Manufacturing Test



Is this better solved with Automated Test Equipment technology, or with Design (for Test, Built-In Self-Test) ?

Is this even solvable with ATE technology alone?

Analogy #2

- ITRS technologies are like parts of the car
- Every one takes the “engine” point of view when it defines its requirements
  - “Why, you may take the most gallant sailor, the most intrepid airman, the most audacious soldier, put them at a table together – what do you get? The sum of their fears.” - Winston Churchill
- All parts must work together to make the car go smoothly
- (Design = Steering wheel and/or tires … but has never “squeaked” loudly enough)
- Need “global optimization” of requirements

How to Share Red Bricks

- Cost is the biggest missing link within the ITRS
  - Manufacturing cost (silicon cost per transistor)
  - Manufacturing NRE cost (mask, probe card, …)
  - Design NRE cost (engineers, tools, integration, …)
  - Test cost
  - **Technology development cost** → who should solve a given red brick wall?
- Return On Investment (ROI) = Value / Cost
  - Value needs to be defined (“design quality”, “time-to-market”)
- Understanding cost and ROI allows sensible sharing of red bricks across industries

2001 Big Picture

- Message: Cost of Design threatens continuation of the semiconductor roadmap
  - New Design cost model
  - Challenges are now Crises
- Strengthen bridge between semiconductors and applications, software, architectures
  - Frequency and bits are not the same as efficiency and utility
  - New System Drivers chapter, with productivity and power foci
- Strengthen bridges between ITRS technologies
  - Are there synergies that “share red bricks” more cost-effectively than independent technological advances?
  - “Manufacturing Integration” cross-cutting challenge
  - “Living ITRS” framework to promote consistency validation

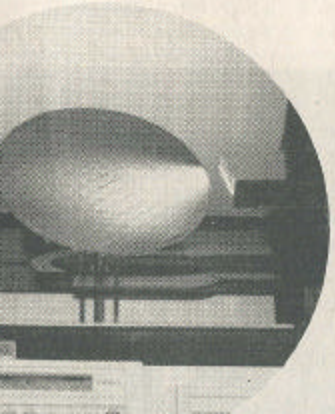
intel.com

Will Moore's Law stand forever?

In 1965, Intel's Gordon Moore created a "law" that became shorthand for the rapid, unprecedented growth of technology. He predicted that the number of transistors on a chip would grow exponentially

to fulfill Moore's Law, year
after year, companies everywhere
can do more at lower cost.
And that's not just a good law.

It's very good business.



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THANK YOU !

PIDS (Devices/Structures)

- CV/I trend (17% per year improvement) = “constraint”
- Huge increase in subthreshold I_{off}
  - Room temperature: increases from 0.01 uA/um in 2001 to 10 uA/um at end of ITRS (22nm node)
    - At operating temperatures (100 – 125 deg C), increase by 15 - 40x
  - Standby power challenge
    - Manage multi-V_t, multi-V_{dd}, multi-Tox in same core
    - Aggressive substrate biasing
    - Constant-throughput power minimization
    - Modeling and controls passed to operating system and applications
- Aggressive reduction of Tox
  - Physical Tox thickness < 1.4nm (down to 1.0nm) starting in 2001, even if high-k gate dielectrics arrive in 2004
  - Variability challenge: “10%” < one atomic monolayer

Assembly and Packaging

- Goal: cost control ($0.07/pin, $2 package, …)
- "Grand Challenge" for A&P: work with Design to develop die-package co-analysis, co-optimization tools
- Bump/pad counts scale with chip area only
  - Effective bump pitch roughly constant at 300um
  - MPU pad counts flat from 2001-2005, but chip current draw increases 64%
- IR drop control challenge
  - Metal requirements explode with I_{chip} and wiring resistance
- Power challenge
  - 50 W/cm^2 limit for forced-air cooling; MPU area becomes flat because power budget is flat
  - More control (e.g., dynamic frequency and supply scaling) given to OS and application
  - Long-term: Peltier-type thermoelectric cooling, …→ design must know

Manufacturing Test

- High-speed interfaces (networking, memory I/O)
  - Frequencies on same scale as overall tester timing accuracy
- Heterogeneous SOC design
  - Test reuse
  - Integration of distinct test technologies within single device
  - Analog/mixed-signal test
- Reliability screens failing
  - Burn-in screening not practical with lower Vdd, higher power budgets → overkill impact on yield
- Design challenges: DFT, BIST
  - Analog/mixed-signal
  - Signal integrity and advanced fault models
  - BIST for single-event upsets (in logic as well as memory)
  - Reliability-related fault tolerance

Lithography

- 10% CD uniformity is a red brick today
- 10% < 1 atomic monolayer at end of ITRS
- This year: Lithography, PIDS, FEP agreed to raise CD uniformity requirement to 15% (but still a red brick)
- Design for variability
  - Novel circuit topologies
  - Circuit optimization (conflict between slack minimization and guardbanding of quadratically increasing delay sensitivity)
  - Centering and design for $/wafer
- Design for when devices, interconnects no longer 100% guaranteed correct?
  - Potentially huge savings in manufacturing, verification, test costs

Figure of Merit for LNAs

LNA performance:

- *dynamic range*
- *power consumption*

$$FOM_{LNA} = \frac{G \cdot IIP3 \cdot f}{(NF - 1) \cdot P}$$

G	gain
NF	noise figure
IIP3	third order intercept point
P	dc supply power
f	frequency

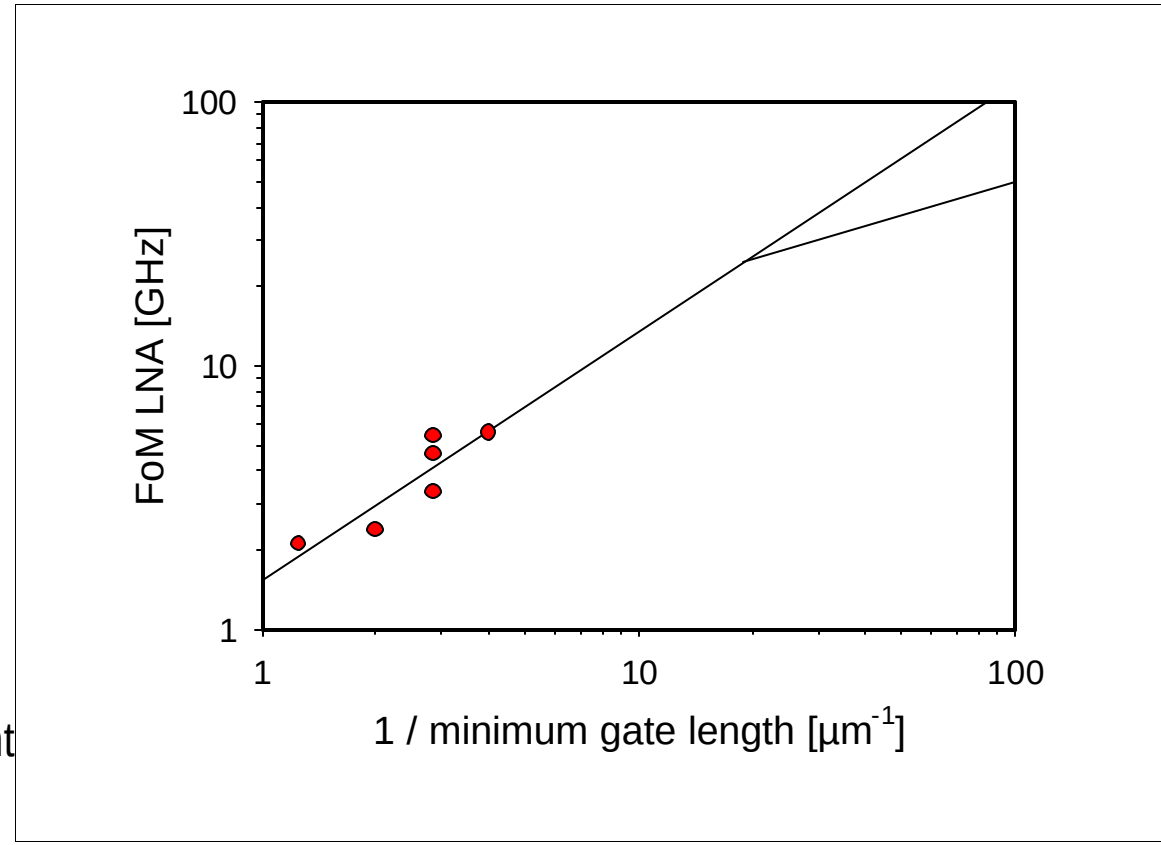


Figure of Merit for ADCs

ADC performance:

- *dynamic range*
- *bandwidth*
- *power consumption*

$$FoM_{ADC} = \frac{\left(2^{ENOB_0}\right) \times \min(\{f_{sample}\}, \{2 \times ERBW\})}{P}$$

$ENOB_0$	effective number of bits
f_{sample}	sampling frequency
$ERBW$	effective resolution bandwidth
P	supply power

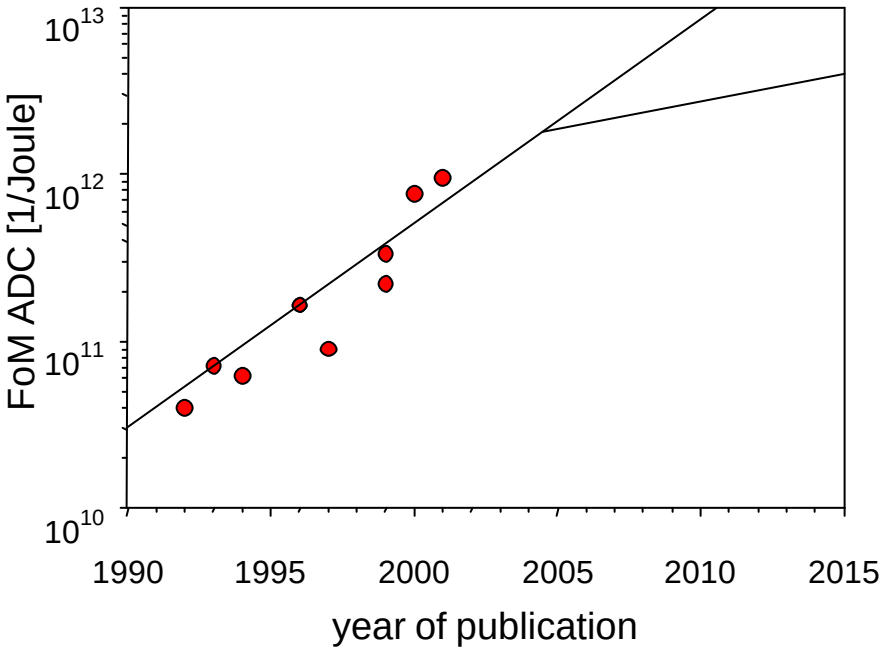


Figure of Merit for VCOs

VCO performance:

- *timing jitter*
- *power consumption*

$$FoM_{VCO} = \left(\frac{f_0}{\Delta f} \right)^2 \frac{1}{L\{\Delta f\} \cdot P}$$

f_0	carrier frequency
Df	frequency offset from f_0
L{Df}	phase noise
P	supply power

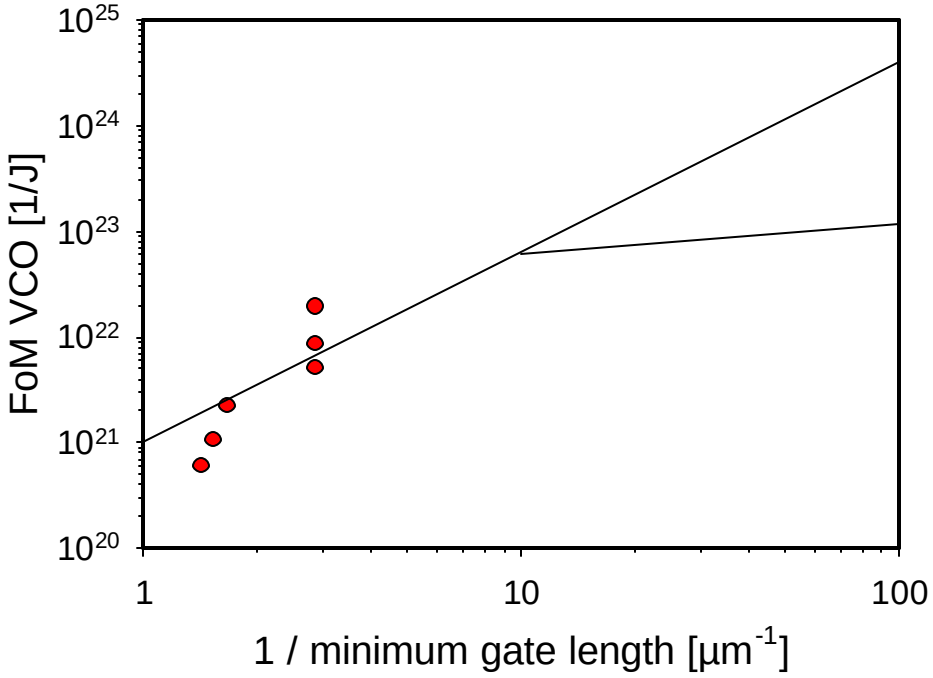


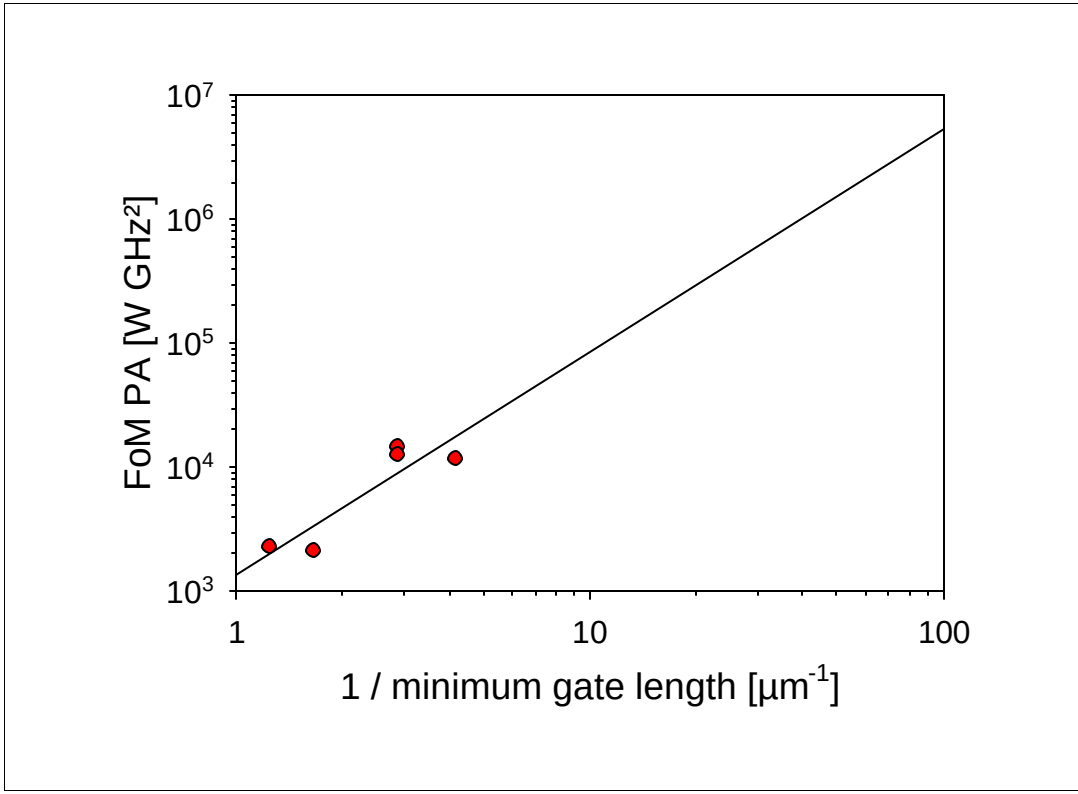
Figure of Merit for PAs

PA performance:

- *output power*
- *power consumption*

$$FoM_{PA} = P_{out} \cdot G \cdot PAE \cdot f^2$$

P_{out}	output power
G	gain
PAE	power added efficiency
$IIP3$	third order intercept point
f	frequency



Mixed-Signal Device Parameters

(1)	Year of Production		2001	2002	2003	2004	2005	2006	2007	OWNER
	DRAM Pitch (Sc 2.0) (nm)		130	115	100	90	80	70	65	ORTC
	MPU Pitch (Sc 3.7) (nm)		150	130	105	90	80	70	65	ORTC
	MPU Printed Gate Length (Sc 3.7) (nm)		90	75	65	53	45	40	35	ORTC
	MPU Physical Gate Length (Sc 3.7) (nm)		65	53	45	37	32	30	25	ORTC
	ASIC/Low Power Pitch (Sc 3.x) (nm)									ORTC
	ASIC/Low Power Printed Gate Length (Sc 3.x) (nm)		100	90	80	70	65	55	50	ORTC
	ASIC/Low Power Physical Gate Length (Sc 3.x) (nm)		90	80	70	65	60	50	45	ORTC
(2)	Minimum Supply Voltage	Digital Design (V)	0.9-1.3	0.8-1.2	0.8-1.1	0.7-1.0	0.6-0.9	0.55-0.8	0.5-0.7	PIDS
(3)		Analog Design (V)	3.3-1.8				2.5-1.8			Design
(14)	nMOS RF Device	Tox (nm)	1.2-1.5	1.0-1.5	1.0-1.4	0.9-1.3	0.8-1.2	0.7-1.0	0.6-0.8	PIDS
(15)		fmax (GHz)	50	55	60	65	70	75	80	Design
(16)		ft (GHz)	95	105	120	130	140	170	190	PIDS
(17)		Gm / Gds @Lmin-digital	20	20	20	20	20	20	20	Design
(18)		@10 Lmin-digital	100	100	100	100	100	100	100	Design
(19)		1/f Noise ($\mu V^2\ \mu m^2$ / Hz)	500	500	300	300	300	200	200	Design
(20)		3 Vth matching (mV µm)	15	15	15	12	12	9	9	Design
(21)	nMOS Analog Device	Tox (nm)	7-2.5	7-2.5	5-2.5	5-2.5	5-2.5	5-2.5	5-2.5	PIDS
(22)		Analog Vth (V)	0.5-0.3	0.5-0.2	0.5-0.2	0.5-0.2	0.4-0.2	0.4-0.2	0.4-0.2	Design
(23)		Gm / Gds @10 Lmin-digital	200	200	200	200	200	200	200	Design
(24)		1/f Noise ($\mu V^2\ \mu m^2$ / Hz)	1000	500	500	500	300	300	300	Design
(25)		3 Vth matching (mV µm)	21	21	15	15	15	15	15	Design
(26)	Analog Capacitor	Density (fF/µm ^{2})	2 3	3 3	4 4	4				Design
(27)		Q (1 / k ^{2} µm^2 GHz)	200	300	300	300	450	450	450	Design
(28)		Voltage linearity (ppm / V^2)	100	100	100	100	100	100	100	Design
(29)		Leakage (fA / [pF V])	7 7	7 7	7 7	7				Design
(30)		3 Matching (% µm^2)	4.5	3	3	3	2.5	2.5	2.5	Design
(34)	Resistor	Resistance (/)	100	100	100	100	100	100	100	Design
(35)		Q (k ^{2} µm^2 GHz)	1000	1500	1500	1500	2000	2000	2000	Design
(36)		Temp. linearity (ppm / C)	60	60	50	50	50	40	40	Design
(37)		3 Matching (% µm)	9 8	8 8	7 7	7				Design
(38)		1/f current noise per current^2 (1 / [µm^2 Hz])	10^{-18}	10^{-18}	10^{-18}	10^{-18}	10^{-18}	10^{-18}	10^{-18}	Design
(39)	Inductor	Density (nH/µm ^{2})	0.03	0.03	0.03	0.03	0.03	0.03	0.03	Design
(40)		Q_{3dB}	12	15	17	18	19	20	20	Design
(41)	Signal Isolation	S21 (dB)	-100	-100	-100	-100	-120	-120	-120	PIDS

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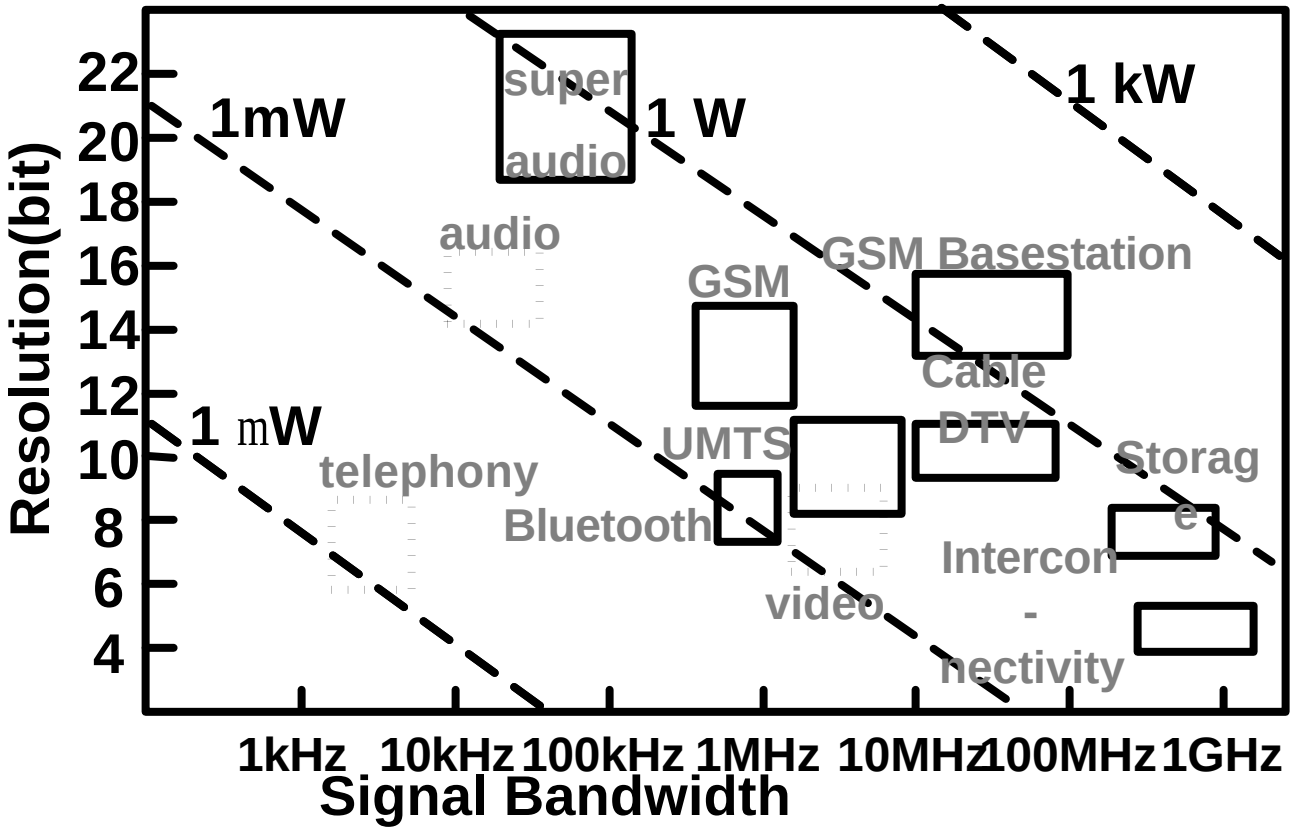
Mixed-Signal Market Drivers



System drivers for mass markets can be identified from the FoM approach

High Performance Table

ITRS 2001 ASIC-HP										
	Near Term							Long Term		
Calendar Year	*2001*	*2002*	*2003*	*2004*	*2005*	*2006*	*2007*	*2010*	*2013*	*2016*
Technology Node	*130nm*			*90nm*			*65nm*	*45nm*	*32nm*	*22nm*
Ph. GL (nm)	65	53	45	37	32	28	25	18	13	9
EOT (nm)	1.3-1.6	1.2-1.5	1.1-1.6	0.9-1.4	0.8-1.3	0.7-1.2	0.6-1.1	0.5-0.8	0.4-0.6	0.4-0.5
Elec. Thick. Adjust. Factor	0.8	0.8	0.8	0.8	0.8	0.8	0.5	0.5	0.5	0.5
Vdd (V)	1.2	1.1	1.0	1.0	0.9	0.9	0.7	0.6	0.5	0.4
Ioff (uA/um)	0.01	0.03	0.07	0.1	0.3	0.7	1	3	7	10
Ion (uA/um)	900	900	900	900	900	900	900	1200	1500	1500
Tech. Improvement	0	0	0	0	0	0	0	30%	70%	100%
Parasitic S/D Rsd (ohm-um)	190	180	180	180	180	170	140	110	90	80
Parasitic S/D Rsd percent (Vdd/Idd)	16%	16%	17%	18%	19%	19%	20%	25%	30%	35%
CV/I (ps)	1.65	1.35	1.13	0.99	0.83	0.76	0.68	0.39	0.22	0.15
Device Performance	1.0	1.2	1.5	1.6	2.0	2.1	2.5	4.3	7.2	10.7
Energy of Switching Transition (fJ/Device)	0.347	0.212	0.137	0.099	0.065	0.052	0.032	0.015	0.007	0.002
Static Power Dissipat. (Watts/Device)	6E-09	7E-09	1E-08	1E-08	3E-08	5E-08	5E-08	1E-07	1E-07	1E-07

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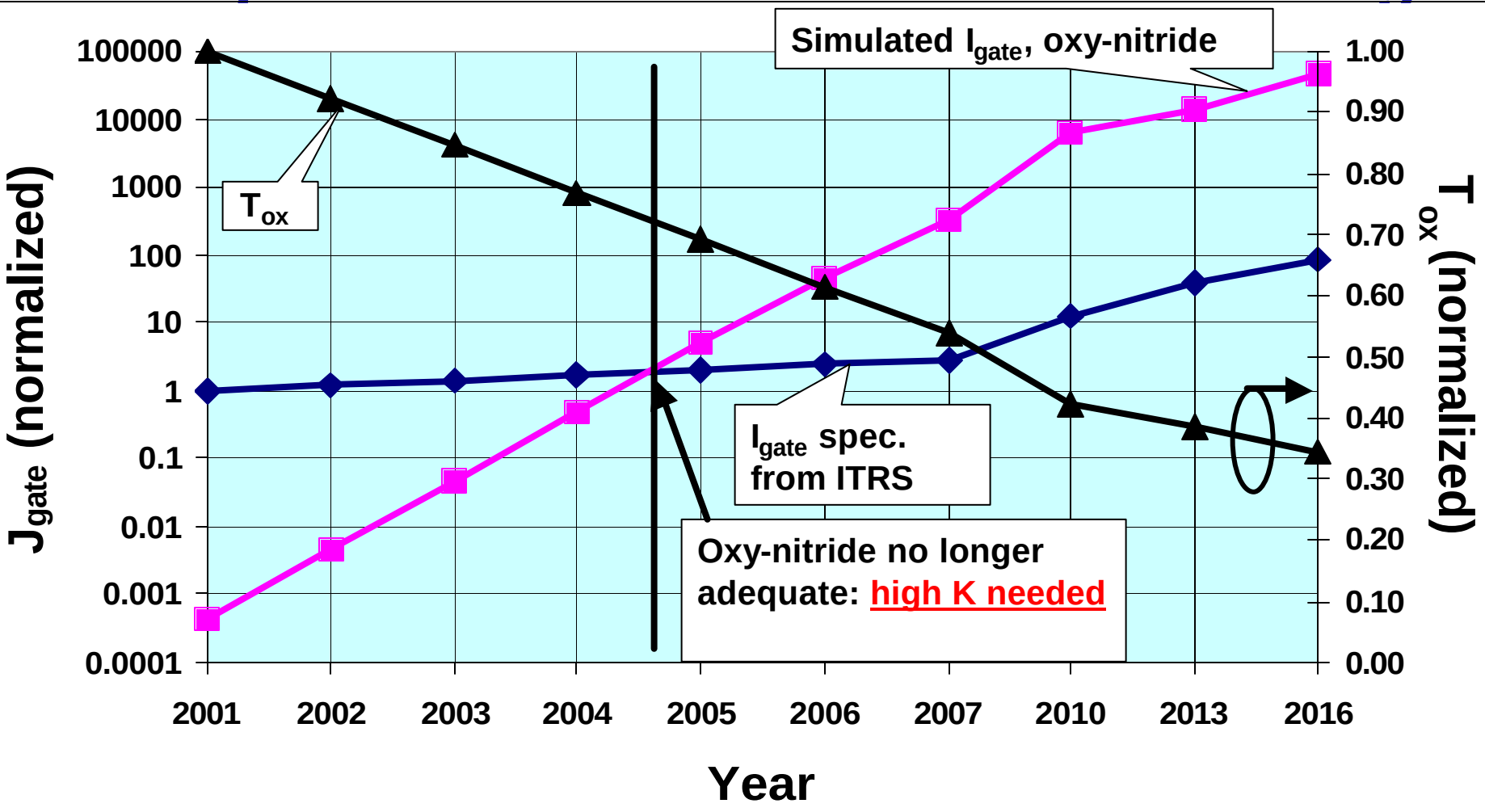
ITRS Projections for Low Power Gate Leakage



- Need for high K driven by Low Power, not High Performance

Emerging Research Devices
Requirements & Motivations for Beyond CMOS

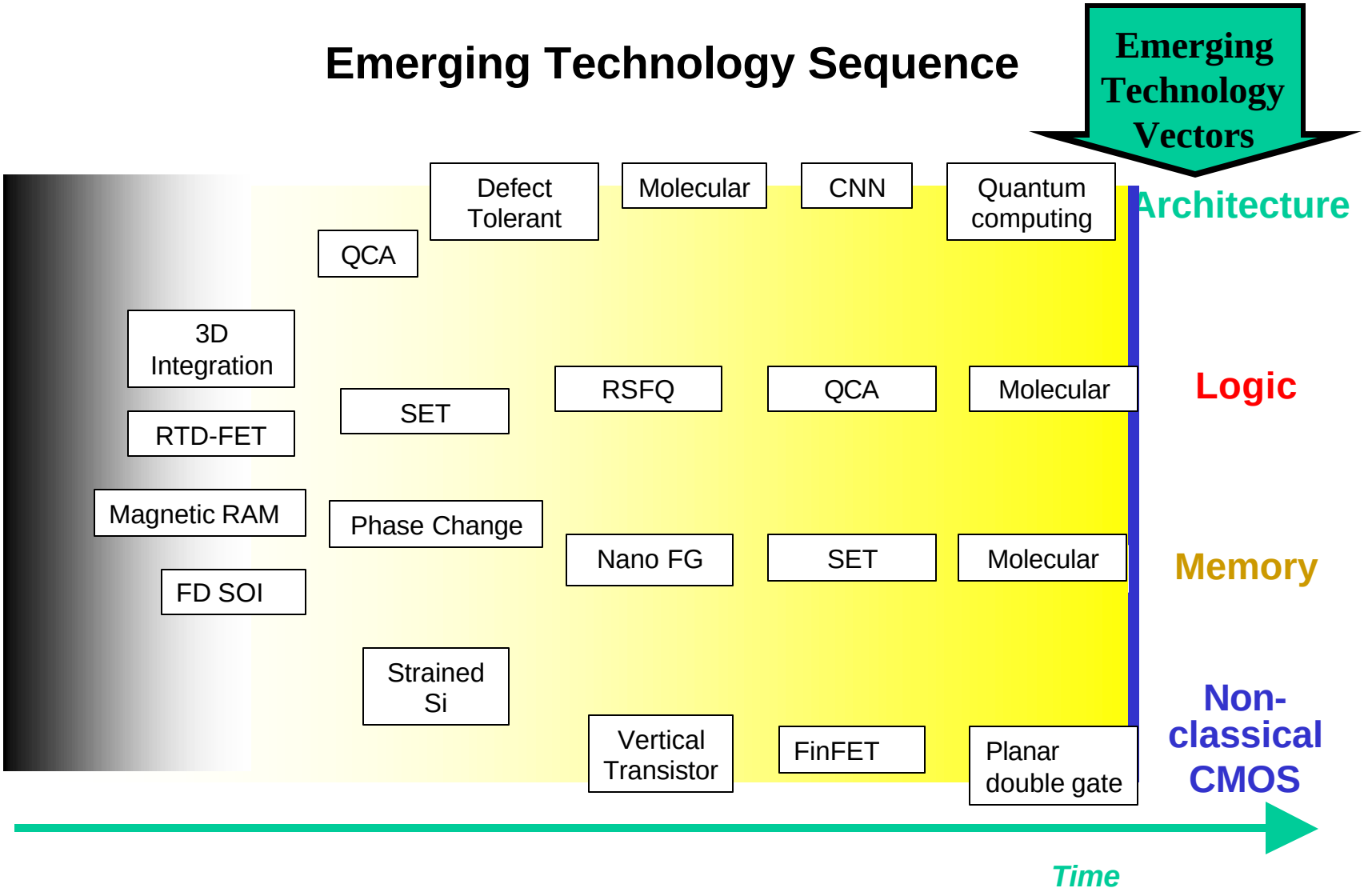
Fundamental Requirements (partial list)

- Energy restorative functional process (e.g. gain)
- Extend microelectronics beyond the domain of CMOS

Compelling Motivations (or-ed)

- Functionally scaleable > 100x beyond CMOS limit
- **or** High information processing rate and throughput
- **or** Minimum energy per functional operation
- **or** Minimum, scaleable cost per function or
- **or** Interfaceable with CMOS.

Emerging Technology Sequence



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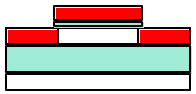
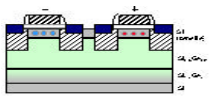
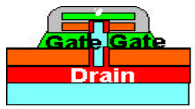
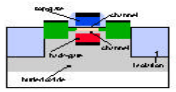
Non - Classical CMOS

					
Device	*Ultra-Thin Body SOI*	*Band-Engineered Transistor*	*Vertical Transistor*	*FinFET*	*Double-Gate Transisto*
Concept	**Fully depleted SOI**	**SiGe or Strained Si channel; bulk Si or SOI**	**Double-gate or surround-gate structure (No specific temporal sequence for these three structures is intended)**		
Application/driver	**Higher performance, Higher transistor density, Lower power dissipation**				
Advantages	**-Improved subthreshold slope –V_t controllability**	**-Higher drive current -Compatible with bulk and SOI CMOS**	**-Higher drive current Lithography independent L_g**	**-Higher drive current -Improved subthreshold slope -Improved short channel effect -Stacked NAND**	**-Higher drive current -Improved subthreshold slope -Improved short channel effect -Stacked NAND**
Scaling Issues	**-Si film thickness -Gate stack -Worse short channel effect than bulk CMOS**	**-High mobility film thickness, in case of SOI -Gate stack -Integration**	**-Si film thickness -Gate stack -Integrability -Process complexity -Accurate TCAD including QM**	**-Si film thickness -Gate stack -Process complexity -Accurate TCAD including QM effect**	**-Gate alignment -Si film thickness -Gate stack -Integrability -Process complexity -Accurate TCAD including QM effect**
Design Challenges	**-Device characterization -Compact model and parameter extraction**	**-Device characterization**	**-Device characterization -PD versus FD -Compact model and parameter extraction -Applicability to mixed signal applications**		
Maturity	**Development**				
Timing	**Near Future** →				

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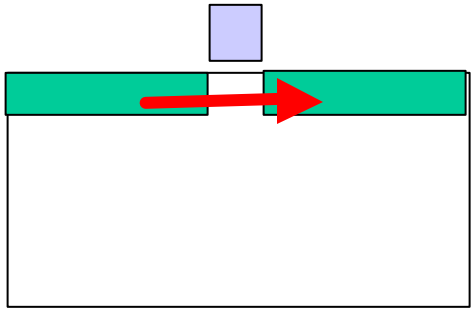
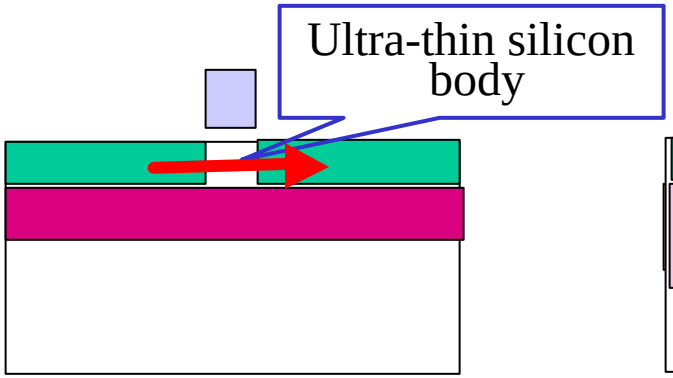
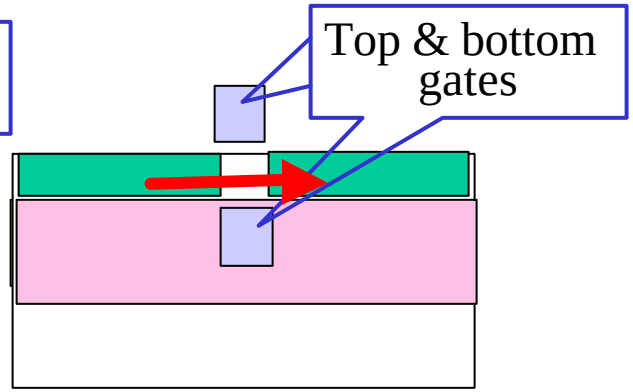
Cross-sections of Non-Classical CMOS Devices



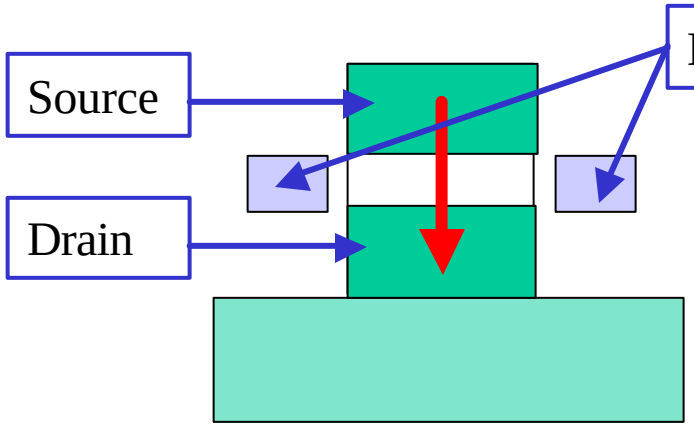
Bulk MOSFET



Ultra-Thin Body MOSFET



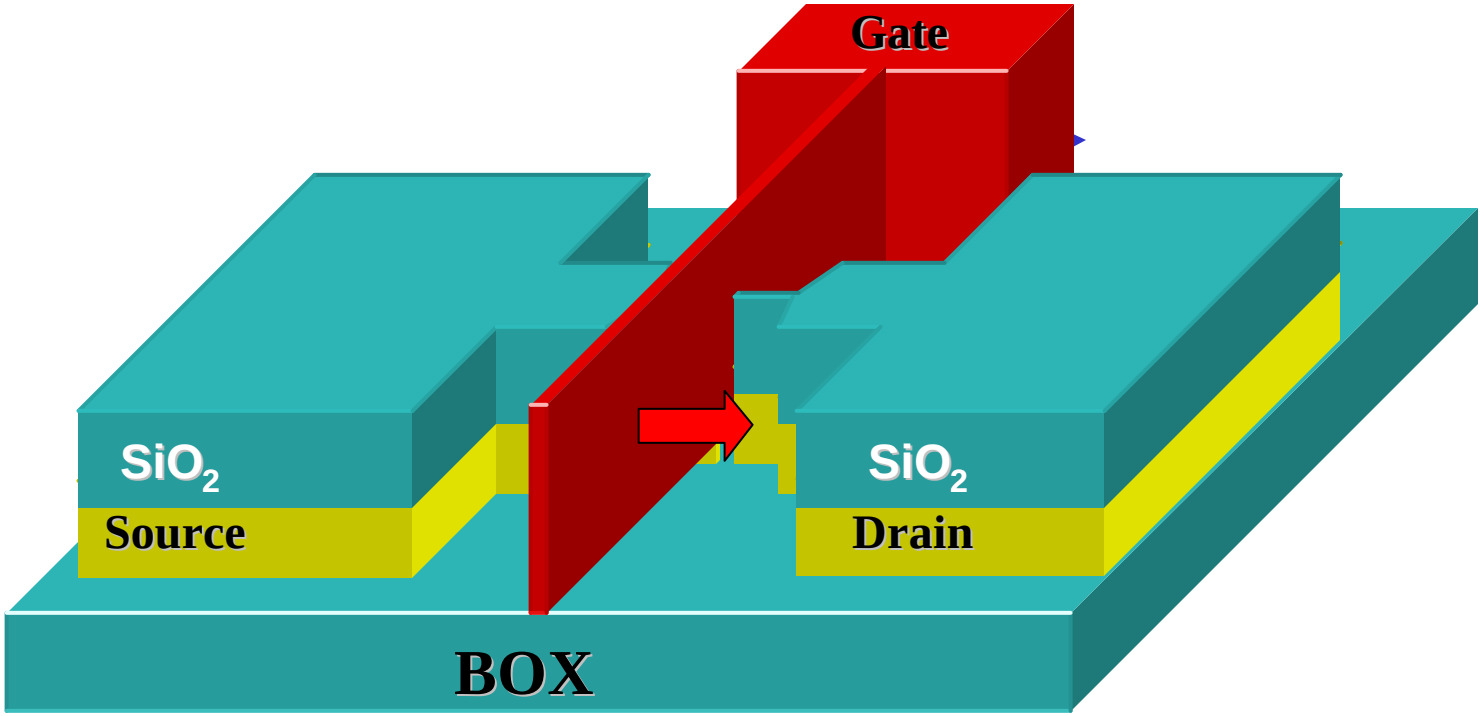
Double-Gate MOSFET



Vertical MOSFET

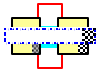
Electron Current Flow

Cross-sections of Non-Classical CMOS Devices



FinFET

Emerging Research Memory Devices

STORAGE MECHANISM	*BASELINE 2002 TECHNOLOGIES*		*MAGNETIC RAM*		*PHASE CHANGE MEMORY*	*NANO FLOATING GATE MEMORY*	*SINGLE/FEW ELECTRON MEMORIES*	*MOLECULAR MEMORIES*
								
DEVICE TYPES	*DRAM*	*NOR FLASH*	*PSEUDO-SPIN-VALVE*	*MAGNETIC TUNNEL JUNCTION*	*OUM*	*-ENGINEERED TUNNEL BARRIER -NANOCRYSTAL*	*SET*	*-BISTABLE SWITCH -MOLECULAR NEMS -SPIN BASED MOLECULAR DEVICES*
AVAILABILITY	**2002**		**~2004**	**~2004**	**~2004**	**>2005**	**>2007**	**>2010**
GENERAL ADVANTAGES	**Density Economy**	**Non-volatile**	**Non-volatile, High endurance, Fast read and write, Radiation hard, NDRO**		**Non-volatile, Low power, NDRO, Radiation hard**	**Non-volatile, Fast read and write**	**Density Power**	**Density, Power Identical Switches, Larger I/O difference, Opportunities for 3D easier to interconnect defect tolerant circuitry**
CHALLENGES	**Scaling**	**Scaling**	**Integration issues, Material quality, Control magnetic properties for write operations**		**New materials and integration**	**Material Quality**	**Dimensional Control (Room temperature operation), Background Charge**	**Volatile Thermal Stability**
MATURITY	**Production**		**Development**		**Development**	**Demonstrated**	**Demonstrated**	**Demonstrated**

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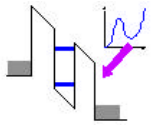
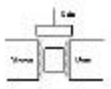
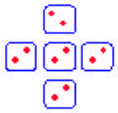
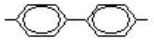
Emerging Research Logic Devices[1]

						
DEVICE	RESONANT TUNNELING DIODE – FET	SINGLE ELECTRON TRANSISTOR	RAPID SINGLE QUANTUM FLUX LOGIC	QUANTUM CELLULAR AUTOMATA	NANOTUBE DEVICES	MOLECULAR DEVICES
TYPES	**3-terminal**	**3-terminal**	**Josephson Junction +inductance loop**	**-Electronic QCA -Magnetic QCA**	**FET**	**2-terminal and 3-terminal**
ADVANTAGES	**Density, Performance, RF**	**Density, Power, Function**	**High speed, Potentially robust, (insensitive to timing error)**	**High functional density, No interconnect in signal path, Fast and low power**	**Density, Power**	**Identity of individual switches (e.g., size, properties) on sub-nm level. Potential solution to interconnect problem**
CHALLENGES	**Matching of device properties across wafer**	**New device and system, Dimensional control (e.g., room temp operation), Noise (offset charge), Lack of drive current**	**Low temperatures, Fabrication of complex, dense circuitry**	**Limited fan out. Dimensional control (room temperature operation), Architecture, Feedback from devices, Background charge**	**New device and system, Difficult route for fabricating complex circuitry**	**Thermal and environmental stability, Two terminal devices, Need for new architectures**
MATURITY	**Demonstrated**	**Demonstrated**	**Demonstrated**	**Demonstrated**	**Demonstrated**	**Demonstrated**

[1]The time horizon for entries increases from left to right in these tables

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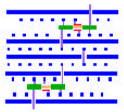
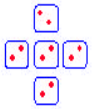
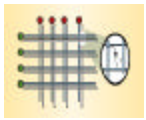
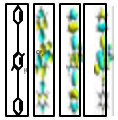
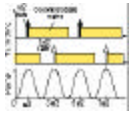
Emerging Research Architectures

						
Architecture	3-D Integration	Quantum Cellular Automata	Defect Tolerant Architecture	Molecular Architecture	Cellular Nonlinear Networks	Quantum Computing
Device Implementation	**CMOS with dissimilar material systems**	**Arrays of quantum dots**	**Intelligently assembles nanodevices**	**Molecular switches and memories**	**Single electron array architectures**	**Spin resonance transistors, NMR devices, Single flux quantum devices**
Advantages	**Less interconnect delay, Enables mixed technology solutions**	**High functional density. No interconnects in signal path**	**Supports hardware with defect densities >50%**	**Supports memory based computing**	**Enables utilization of single electron devices at room temperature**	**Exponential performance scaling, Enables unbreakable cryptography**
Challenges	**Heat removal, No design tools, Difficult test and measurement**	**Limited fan out, Dimensional control (low temperature operation), Sensitive to background charge**	**Requires pre-computing test**	**Limited functionality**	**Subject to background noise, Tight tolerances**	**Extreme application limitation, Extreme technology**
Maturity	**Demonstration**	**Demonstration**	**Demonstration**	**Concept**	**Demonstration**	**Concept**

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