Large-scale Nano-PLA Meshes with Efficient Logic Mapping

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Abstract. An area efficient architecture for organization of sublithographic PLAs(Programmable Logic Arrays) is proposed. We also suggest three different algorithms for efficient logic mapping on this architecture, namely the Max-Clique Partitioning, Repeated Min-Cut, and Multi-level Construction via Coarse Graphs. Each of the algorithms is presented in different individual and independent sections in this report. Comparisons are made with existing algorithms on benchmark circuits where necessary.

1 Architecture

Recent advances in molecular electronics [20] [10] and sub-lithographic Nano-architectures of FPGAs(Field Programmable Gate Arrays) [4] [9] [25] has reaffirmed the belief that nanotechnology will extend the Moore's Law [21] in this new century [14] [22]. Most of these nano-architectures [1] [5] [6] [24] are crossbar structures because of their ease of fabrication and support for defect tolerance. This paper envisions an architecture for full-scale electronic systems based on the crossbar approach.

We organize the nano-PLAs into nano-PLA blocks and further group them into nano-PLA clusters. These nano-PLA clusters form the building blocks of reconfigurable nano-electronic devices similar to the existing lithographic CPLDs (Complex Programmable Logic Devices). Because of the bottom-up fabrication techniques used to make these nano-electronic devices, they will have interconnect requirements very different [6] from the existing CPLDs [7]. Their efficiency would closely depend on the logic mapping technique used to embed logic onto them.

2 Max-Clique Partitioning

Traditionally, logic mapping techniques in VLSI design literature have been divided into two classes - the Bottom-up Clustering and the Recursive Top-down Partitioning [19]. The Top-down partitioning methods [17] [8] [26] divide a circuit into smaller and more manageable components. The Bottom-up clustering methods [2] [11] [23] look at the problem of circuit logic break-up from the view of grouping together elements to form circuit clusters. While top-down methods fail in cases when the circuits are large because of their complexity, bottom-up fail because of their lack of reliance on the global view of the circuit. The algorithm proposed banks on the strengths of both these methods and in that sense is a hybrid of the two.

Recent developments in graph heuristics for maximum clique search [3] [16] are the motivation of the proposed algorithm. These heuristics are used to find the maximum clique in the adjacency graph of the netlist for a circuit. This clique is removed clique and the maximum clique in the residual graph is searched and so on. The partitions so obtained are unbalanced and we balance them using bottom-up techniques based on density criterions.

3 Min-Cut based Partitioning

We are considering the problem of partitioning a graph into subgraphs of constant size, with the minimum possible interconnect between the partitions. This problem is known to be NP-Hard even in the case of two partitions (this is called bipartitioning). However, several heuristics have been developed for efficient approximations of bipartitioning [13] [27] [12] [18]. On the other hand, other approximations take a more bottom up approach [2] [11] [23]. We implemented a bottom up max-clique based heuristics. This however, is slow on large inputs, and gives better results on denser graphs, where there are large cliques of which to take advantage. Thus we get better results by first applying a min-cut based heuristics on the large input, and then the bottom up max-cut based heuristics on the smaller, denser subgraphs created as partitions by the min-cut heuristics. The min-cut heuristics we implemented is based on the paper [27] on bipartitioning. The technique used in [27] is to construct a network flow from our graph, such that a min-cut in the network flow will correspond to a min-net-cut in the graph. Although a min-net-cut is not optimal, it will be a good approximation.

4 Multi-level Partitioning via Coarse Graphs

A mesh of nanowires with PLAs at particular junctions can be logically programmed to fit logic functions. However, doing this efficiently is a problem, since looking at all possible combinations is a lengthy process. We work to solve this situation by reducing the nanomesh into a graph. The algorithm that I use is a multilevel algorithm for partitioning generic graphs proposed by Bruce

Hendrickson and Robert Leland of the Sandia National Laboratories [15]. The algorithm can be generalized as this: it breaks down a given graph into smaller and smaller graphs (hence the "multilevel"). This breakdown is accomplished using coarsening methods. Once it is small enough, the graph is partitioned (using a spectral method, although others can be substituted). Then, the graph in question and the partitions are uncoarsened until the original graph is achieved. As the number of possible partitions grows exponentially with the size of the vertex set, a maximal partition of the coarse graph is faster than a partition of the original graph. Obviously, the main setback is that "only a small number of the possible fine graph partitions are represented" and examined on the coarse graph [15].

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