

Adiabatic Logic

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1 Adiabatic Logic

Adiabatic Logic is the term given to low-power electronic circuits that implement reversible logic. The term comes from the fact that an adiabatic process is one in which the total heat or energy in the system remains constant. Research in this area has mainly been fueled by the fact that as circuits get smaller and faster, their energy dissipation greatly increases, a problem that adiabatic circuits promises to solve.

Most research has focused on building adiabatic logic out of CMOS. However, current CMOS technology, though fairly energy efficient compared to similar technologies, dissipate energy as heat, mostly when switching. In order to solve this problem, there are two fundamental rules CMOS adiabatic circuits must follow, the reasons for which are explained below. The first is never to turn on a transistor when there is a voltage difference between the drain and source. The second says never to turn off a transistor that has current flowing through it.

Several designs of adiabatic CMOS circuits have been developed. Some of the more interesting ones include Split-level Charge Recovery Logic (SCRL) [1] and Two Level Adiabatic Logic or 2LAL [2]. Both rely heavily on the transmission gates, use trapezoidal waves to clock the circuit and can be fully pipelined.

Of interest is also adiabatic circuits built using current nanomaterials such as silicon nanowires or carbon nanotubes since nanoelectronics are expected to dissipate a great amount of heat.

1.1 Adiabatic Logic out of CMOS circuits

CMOS transistors dissipate power when they switch. The main part of this dissipation is due to the need to charge and discharge the gate capacitance C through a component that has some resistivity R . The energy dissipated when

charging of the gate is

$$E = \frac{RC}{T} \cdot CV^2$$

Where T is the time it takes the gate to charge or discharge. In non-reversible circuits, the charging time T is proportional to RC . Reversible logic uses the fact that a single clock cycle is much longer than RC and thus attempts to spread the charging of the gate over the whole cycle and thus reduces the energy dissipated. In order to extend the charging time of the gate we make sure never to turn on a transistor that has a potential difference between source and drain, and furthermore, once the transistor is turned on, energy flows through it in a gradual and controlled manner.

The second rule that adiabatic circuits must follow is never to turn off a transistor when there is current flowing through it. The reason for this follows from the fact that transistors are not perfect switches going from on to off instantly. Instead, it gradually changes from on to off when the gate voltage changes. Furthermore, the change is proportional to the speed at which the gate voltage changes. A fact that when combined with the previous constraint, implies that the transistor is in an “in between” state for a long period of time. During this time, the voltage drop across the transistor greatly increases yet the resistance is not high enough to bring power dissipation to zero.

1.1.1 SCRL

Knight and Younis [1] developed a family of adiabatic circuits known as Split-level Charge Recovery Logic or SCRL. Analyzing a full cycle of the SCRL NAND presented in figure 1 gives a good understanding of how this family of logic works in general.

This circuit is very similar to a conventional NAND; however, one of the main differences is that the top and bottom rails are driven by trapezoidal clocks (Φ_1 and $/\Phi_1$) rather than V_{dd} and G_{nd} . In the beginning the whole circuit is set at $V_{dd}/2$ except for $P1$ which is set to G_{nd} and $/P1$ which is set to V_{dd} so that the transmission gate is off. In the next step, the transmission gate is turned on by gradually switching the value of $P1$ and $/P1$. Following, Φ_1 and $/\Phi_1$ which were at $V_{dd}/2$ are split to V_{dd} and G_{nd} respectively. At this point, the gate computes the NAND of a and b like a non-adiabatic gate would. Once the output is used by the next gate, the transmission gate can be turned back off gradually. Then Φ_1 and $/\Phi_1$ are gradually returned to $V_{dd}/2$ and now the input can change and the next cycle can begin. It is important not to change the input until the rails are back to $V_{dd}/2$ so that a transistor is not turned on when there is a potential difference thus violating the first rule.

The last part that needs explaining is the extra P-MOS connected to input B. Lets analyze what happens when that transistor is missing. Once Φ_1 and

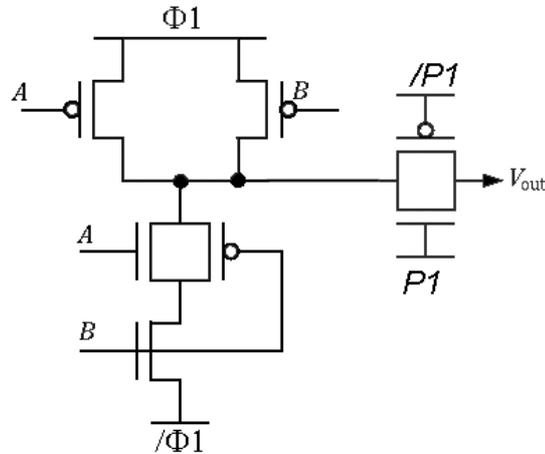


Figure 1: SCRL NAND

$/\Phi 1$ are split, when a has a value of logical 1 and b of logical 0, current flows from V_{dd} through the P-MOS controlled by b and down through the N-MOS controlled by a which means that a high voltage is passing through an N-MOS which will thus dissipate energy. This problem is solved by the extra P-MOS and in general care must be taken to ensure that an internal node is not dissipating energy in this way.

Finally the only node that is not restored by the gate is the output. This is so that a fully pipelined circuit at the gate level can be achieved (see [1] for a detailed explanation of how this is done). Also, in order to achieve the gradual swings needed to operate these gates, trapezoidal clock are used so that initially, the voltage is held constant for quarter of a cycle, then gradually gets turned up or down, held constant again, and for the final quarter, is gradually returned to the initial value.

1.1.2 2LAL

Another interesting adiabatic circuit family is the Two Level Adiabatic Logic or 2LAL developed by Frank [2]. Like SCRL, this family can be fully pipelined at the gate level. Figure 2 (a) shows the basic building block of 2LAL, a pair of transmission gates which transmit signal A and \bar{A} respectively both of which are represented by the single “box” on the left. The fact that 2LAL only requires a basic switching device and is not dependent on CMOS makes it ideal for use with new technologies.

Figure 2 (b) shows the basic buffer element of 2LAL which consist of two sets of transmission gates. $\Phi 1$ and $\Phi 0$ are both trapezoidal clocks but $\Phi 1$ is a quarter cycle behind $\Phi 0$. Initially all the nodes are at 0. As the input gradually raises to 1 (if it is 1) or stays at 0, $\Phi 0$ transitions to 1. On the next step, $\Phi 1$ tran-

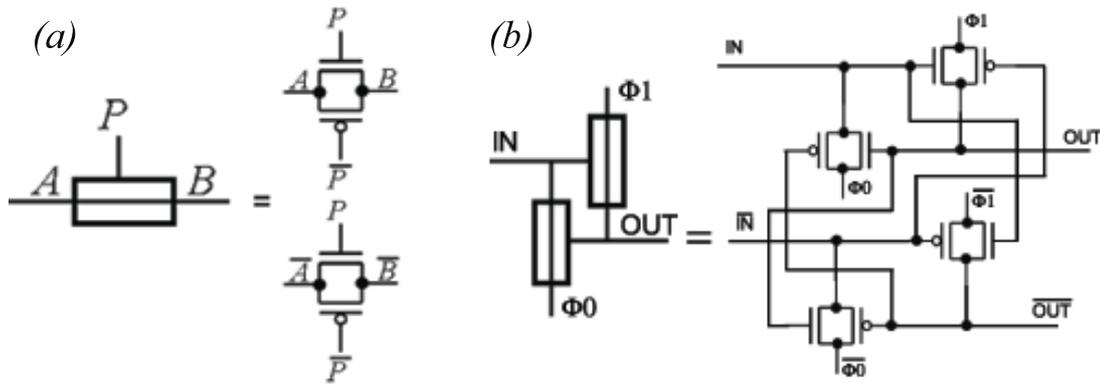


Figure 2: 2LAL Basic Gate (a) and Buffer (b)

sitions to 1 which sets the output to 1 if the input was one and otherwise leaves it at 0 which in itself reduces the power dissipation because no charge passes through the transistor. On the third step Φ_0 transitions back to 0 resetting the input to 0. Finally Φ_1 transitions back to 0 and the output is restored to 0 by the following gate in order to accommodate for full pipelining and thus the circuit is ready to process a new input. Another feature of 2LAL is that inverters can be easily created by simply crossing over the rails when going from one gate to the next.

References

- [1] S. Younis T. Knight, "Asymptotically zero energy computing using split-level charge recovery logic", Technical Report AITR-1500, MIT AI Laboratory June 1994.
- [2] Michael P. Frank, "Physical Limits of Computing. Lecture #24 Adiabatic CMOS", Spring 2002.

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